UNITED STATES DISTRICT COURT
DISTRICT OF DELAWARE

LG.PHILIPS LCD CO., LTD. and LG.PHILIPS LCD AMERICA, INC., Counterclaim Plaintiffs, v. AU OPTRONICS CORPORATION; AU OPTRONICS CORPORATION AMERICA; CHI MEI OPTOELECTRONICS CORPORATION; and CHI MEI OPTOELECTRONICS USA, INC., Counterclaim Defendants.	Civil Action No. 06-726-GMS
AU OPTRONICS CORPORATION, Plaintiff, v. LG.PHILIPS LCD CO., LTD. and LG.PHILIPS LCD AMERICA, INC., Defendants.	Civil Action No. 07-357-GMS **CONSOLIDATED CASES** **JURY TRIAL DEMANDED**

LG.PHILIPS LCD CO., LTD.'S FIRST AMENDED ANSWER TO AU OPTRONICS CORPORATION'S AMENDED COUNTERCLAIMS AND ADDITIONAL COUNTERCLAIMS

LG.Philips LCD Co., Ltd. ("LPL"), by and through its undersigned counsel, hereby files its First Amended Answer to the Amended Counterclaims of Plaintiff AU Optronics Corporation ("AUO"), in the above titled action (C.A. No. 07-357), filed on or about July 10, 2007 (D.I. 93), asserts affirmative defenses to those claims, and asserts additional counterclaims against AUO. A jury trial is demanded for all claims so triable.

RESPONSE TO ALLEGATIONS AS TO THE COUNTERCLAIM PARTIES

1. LPL admits that AUO is a corporation organized under the laws of the Republic of China with its principal place of business in Taiwan as alleged in paragraph 56 of the Counterclaims.

2. LPL lacks knowledge or information sufficient to admit or deny the allegations of paragraph 57 of the Counterclaims and therefore denies them.

3. LPL admits the allegations of paragraph 58 of the Counterclaims.

4. LPL denies the allegations of paragraph 59 of the Counterclaims.

5. LPL admits the allegations of paragraph 60 of the Counterclaims.

6. The allegations in paragraph 61 of the Counterclaims are conclusions of law to which no response is required.

7. The allegations in paragraph 62 of the Counterclaims are conclusions of law to which no response is required.

RESPONSE TO ALLEGATIONS AS TO JURISDICTION AND VENUE

8. LPL admits that this Court has jurisdiction over these Counterclaims, but the remaining allegations of paragraph 63 of the Counterclaims are conclusions of law to which no response is required.

9. LPL admits that this Court has jurisdiction over these Counterclaims, but the remaining allegations of paragraph 64 of the Counterclaims are conclusions of law to which no response is required.

10. LPL admits the allegations of paragraph 65 of the Counterclaims.

RESPONSE TO COUNTERCLAIM COUNT ONE

11. LPL admits that Exhibit A to the Counterclaims purports to be a copy of United States Patent No. 6,734,944, entitled "Liquid Crystal Display" ("the '944 patent"), but LPL lacks knowledge or information sufficient to admit or deny the remaining allegations of paragraph 66 of the Counterclaims, and therefore denies them.

12. LPL denies the allegations in paragraph 67 of the Counterclaims.

13. LPL denies the allegations in paragraph 68 of the Counterclaims.

14. LPL denies the allegations in paragraph 69 of the Counterclaims.

RESPONSE TO COUNTERCLAIM COUNT TWO

15. LPL admits that Exhibit B to the Counterclaims purports to be a copy of United States Patent No. 7,125,157, entitled "Backlight Unit and Liquid Crystal Display Utilizing the Same" ("the '157 patent"), but LPL lacks knowledge or information sufficient to admit or deny the remaining allegations of paragraph 70 of the Counterclaims, and therefore denies them.

16. LPL denies the allegations in paragraph 71 of the Counterclaims.

17. LPL denies the allegations in paragraph 72 of the Counterclaims.

18. LPL denies the allegations in paragraph 73 of the Counterclaims.

RESPONSE TO COUNTERCLAIM COUNT THREE

19. LPL admits that Exhibit C to the Counterclaims purports to be a copy of United States Patent No. 7,090,506, entitled "Signal Transmission Device Having Flexible Printed Circuit Boards" ("the '506 patent"), but LPL lacks knowledge or information sufficient to admit or deny the remaining allegations of paragraph 74 of the Counterclaims, and therefore denies them.

20. LPL denies the allegations in paragraph 75 of the Counterclaims.

21. LPL denies the allegations in paragraph 76 of the Counterclaims.

22. LPL denies the allegations in paragraph 77 of the Counterclaims.

RESPONSE TO COUNTERCLAIM COUNT FOUR

23. LPL refers and incorporates herein its responses to AUO's allegations in paragraphs 1-10, above, as though fully set forth herein.

24. LPL admits the allegations of paragraph 79 of the Counterclaims.

25. LPL denies the allegations in paragraph 80 of the Counterclaims.

26. LPL denies the allegations in paragraph 81 of the Counterclaims.

27. LPL denies the allegations in paragraph 82 of the Counterclaims.

28. LPL denies the allegations in paragraph 83 of the Counterclaims.

RESPONSE TO COUNTERCLAIM COUNT FIVE

29. LPL refers and incorporates herein its responses to AUO's allegations in paragraphs 1-10 and 23-28, above, as though fully set forth herein.

30. LPL denies the allegations of paragraph 85 of the Counterclaims.

31. LPL denies the allegations in paragraph 86 of the Counterclaims.

32. LPL denies the allegations in paragraph 87 of the Counterclaims.

33. LPL denies the allegations in paragraph 88 of the Counterclaims.

RESPONSE TO COUNTERCLAIM COUNT SIX

34. LPL refers and incorporates herein its responses to AUO's allegations in paragraphs 1-10 and 23-33, above, as though fully set forth herein.

35. LPL admits that the LPL patents relate to, inter alia, thin film transistors having double-layer metal gate structures, but otherwise denies the allegations in paragraph 90 of the Counterclaims.

36. LPL denies the allegations in paragraph 91 of the Counterclaims.

37. LPL admits that an application for patent was filed on October 25, 2001 that became U.S. Patent No. 6,753,127. LPL also admits that during the prosecution of the '127 Patent, the Examiner issued an office action on or about August 14, 2002, citing the Seiki Reference. LPL denies the remaining allegations in paragraph 92 of the Counterclaims.

38. LPL denies the allegations in paragraph 93 of the Counterclaims.

39. LPL denies the allegations of paragraph 94 of the Counterclaims.

40. LPL denies the allegations in paragraph 95 of the Counterclaims.

41. LPL denies the allegations in paragraph 96 of the Counterclaims.

42. LPL admits that the Examiner rejected the original claim 1 of the '274 Patent and that the applicant amended the original claim. LPL denies the remaining allegations in paragraph 97 of the Counterclaims.

43. LPL denies the allegations of paragraph 98 of the Counterclaims.

44. LPL admits that U.S. Application No. 09/243,556 was filed on or about February 2, 1999 ("the '556 Application"), which led to U.S. Patent No. 6,340,610 that issued on January 22, 2002, but denies the remaining allegations in paragraph 99 of the Counterclaims.

45. LPL admits that during the prosecution of the '556 Application, the Examiner rejected the original claim 9 in separate office actions (dated September 6, 2000 and March 29, 2001), but denies the remaining allegations in paragraph 100 of the Counterclaims.

46. LPL denies the allegations in paragraph 101 of the Counterclaims.

47. LPL denies the allegations of paragraph 102 of the Counterclaims.

48. LPL denies the allegations in paragraph 103 of the Counterclaims.

RESPONSE TO ALLEGATIONS AS TO EXCEPTIONAL CASE

49. LPL denies the allegations in paragraph 104 of the Counterclaims.

RESPONSE TO PRAYER FOR RELIEF

50. As to paragraphs A through K of the Prayer For Relief, LPL denies that AUO is entitled to the requested relief.

AFFIRMATIVE DEFENSES

Without conceding that any of the following necessarily must be pleaded as an affirmative defense, or that any of the following are not already at issue by virtue of the foregoing denials, and without prejudice to LPL's right to plead additional defenses as discovery into the facts of the matter warrants, LPL hereby asserts the following affirmative defenses:

FIRST AFFIRMATIVE DEFENSE

51. One or more claims of the Asserted AUO Patents are invalid for failing to meet one or more of the requisite conditions or requirements for patentability specified by 35 U.S.C. §§ 101, 102, 103, and/or 112.

SECOND AFFIRMATIVE DEFENSE

52. LPL's products have not and do not infringe any claim of the Asserted AUO Patents, either literally or under the doctrine of equivalents.

THIRD AFFIRMATIVE DEFENSE

53. LPL has not directly or indirectly contributed to infringement of, nor induced another to infringe the Asserted AUO Patents.

FOURTH AFFIRMATIVE DEFENSE

54. AUO has failed to state a claim for which relief can be granted.

FIFTH AFFIRMATIVE DEFENSE

55. Pursuant to 35 U.S.C. § 287(b), LPL is not liable for damages for infringement under any section of 35 U.S.C. § 271 before receiving notice of AUO's allegations of infringement in this action.

SIXTH AFFIRMATIVE DEFENSE

56. AUO's claims are barred, in whole or in part, because of the affirmative defense of license.

SEVENTH AFFIRMATIVE DEFENSE

57. AUO's '944 Patent is unenforceable due to inequitable conduct, including, but not limited to the allegations set forth in Counterclaim IX below, which are incorporated herein.

ADDITIONAL COUNTERCLAIMS

58. By these Counterclaims and pursuant to Rule 13, Rule 19 and/or Rule 20 of the Federal Rules of Civil Procedure, Defendant/Counterclaim Plaintiff LG.Philips LCD Co., Ltd. ("LPL") seeks injunctive and declaratory relief and damages, including treble or multiple damages against Counterclaim Defendants AU Optronics Corporation ("AUO"), Chi Mei Optoelectronics Corporation ("CMO"), and Chi Mei Optoelectronics USA, Inc. ("CMO USA").

59. Counterclaim Plaintiff LG.Philips LCD Co., Ltd. ("LPL") is a Korean corporation having its head office at 18th Floor, West Tower, LG Twin Towers, 20 Yoido-dong, Youngdungpo-gu, Seoul, Republic of Korea 150-721.

60. Counterclaim Defendant AUO is a Taiwanese corporation, having its principal place of business at 1, Li-Hsin Rd., II, Science-Based Industrial Park, Hsinchu City 30077 Taiwan, ROC.

61. Counterclaim Defendant Chi Mei Optoelectronics Corporation ("CMO") is a Taiwanese corporation, having its principal place of business at 2F, No. 1, Chi-Yeh Road, Tainan Science Based Industrial Park, Hsinshih Hsiang, Tainan Hsien 710, TAIWAN 74147, R.O.C. CMO manufactures LCD products in Taiwan and China and, on information and belief, directs those products to the United States, including Delaware, through established distribution channels involving various third parties, knowing that these third parties will use their respective nationwide contacts and distribution channels to import into, sell, offer for sale, and/or use these products in Delaware and elsewhere in the United States.

62. Counterclaim Defendant Chi Mei Optoelectronics USA, Inc. ("CMO USA") is a Delaware corporation, having its principal pace of business at 101 Metro Drive Suite 510, San Jose, CA 95110. CMO USA markets and sells CMO's products throughout the United States.

63. These Counterclaims are based upon and arise under the Patent Laws of the United States, 35 U.S.C. § 100 *et seq.*, and in particular §§ 271, 281, 283, 284 and 285, and is intended to redress infringement of United States Patent No. 6,664,569 ("the '569 Patent"), United States Patent No. 6,803,984 ("the '984 Patent"), and United States Patent No. 7,218,374 ("the '374 Patent") owned by LPL.

64. These Counterclaims are also under the Declaratory Judgment Act, 28 U.S.C. §§ 2201 and 2202, and the Patent Laws of the United States, based upon an actual

controversy between LPL and AUO regarding the validity and infringement of the claims of the AUO Patents, and is intended to provide appropriate and necessary declaratory relief.

65. This Court has jurisdiction over the subject matter of these Counterclaims pursuant to 28 U.S.C. §§ 1331 and 1338(a).

66. This Court has personal jurisdiction and venue over AUO and CMO USA because, *inter alia*, AUO and CMO USA have submitted itself to the jurisdiction of this Court.

67. This Court has personal jurisdiction over CMO and venue is proper in this judicial district pursuant to 28 U.S.C. §§ 1391 (b) and (c) and (d), and 28 U.S.C. § 1400(b), in that CMO is committing and is causing acts of patent infringement within the United States and within this judicial district, including the infringing acts alleged herein, both directly, through one or more intermediaries, and as an intermediary, and in that CMO has caused and causes injury and damages in this judicial district by acts or omissions outside of this judicial district, including but not limited to utilization of its own distribution channels established in the United States and CMO USA's distribution channels in the United States, as set forth below, to ship a variety of products that infringe the Patents-in-Suit into the United States and into this judicial district while deriving substantial revenue from services or things used or consumed within this judicial district, and will continue to do so unless enjoined by this Court.

68. On December 16, 2003, the '569 Patent, entitled "Liquid Crystal Display Device Array Substrate and Method of Manufacturing the Same," was duly and legally

issued. LPL is the owner by assignment of all rights, title, and interest in and to the '569 Patent. A copy of the '569 Patent is attached as Exhibit A.

69. On October 12, 2004, the '984 Patent, entitled "Method and Apparatus for Manufacturing Liquid Crystal Display Device Using Serial Production Processes," was duly and legally issued. LPL is the owner by assignment of all rights, title, and interest in and to the '984 Patent. A copy of the '984 Patent is attached as Exhibit B.

70. On May 15, 2007, the '374 Patent, entitled "Liquid Crystal Display Device and Method of Manufacturing the Same," was duly and legally issued. LPL is the owner by assignment of all rights, title, and interest in and to the '374 Patent. A copy of the '374 Patent is attached as Exhibit C.

71. LPL owns the '569 Patent, the '984 Patent, and the '374 Patent, and possesses the right to sue and to recover for infringement of the '569 Patent, the '984 Patent, and the '374 Patent.

72. AUO claims to be the owner of the '944 Patent, the '157 Patent, and the '506 Patent.

COUNTERCLAIM COUNT VI
INFRINGEMENT OF THE '569 PATENT

73. LPL hereby incorporates paragraphs 58-72 above as though fully set forth herein.

74. AUO has infringed, and/or induced infringement of the '569 Patent by making, using, causing to be used, offering to sell, causing to be offered for sale, selling, causing to be sold, importing, and/or causing to be imported products that infringe one or more claims of the '569 Patent in this judicial district and elsewhere in the United States.

75. The products that are used, caused to be used, sold, caused to be sold, offered for sale, caused to be offered for sale, imported, and/or caused to be imported by AUO meet each and every limitation of at least one claim of the '569 Patent, either literally or equivalently.

76. LPL has been and will continue to be injured by AUO's past and continuing infringement of the '569 Patent and is without adequate remedy at law.

77. AUO, upon information and belief, infringed and is infringing the '569 Patent with knowledge of LPL's patent rights and without a reasonable basis for believing its conduct is lawful. AUO's infringement has been and continues to be willful and deliberate, and will continue unless enjoined by this Court, making this an exceptional case and entitling LPL to increased damages and reasonable attorneys' fees pursuant to 35 U.S.C. §§ 284 and 285.

COUNTERCLAIM COUNT VII
INFRINGEMENT OF THE '984 PATENT

78. LPL hereby incorporates paragraphs 58-77 above as though fully set forth herein.

79. AUO, CMO, and CMO USA have infringed, and/or induced infringement of the '984 Patent by making, using, causing to be used, offering to sell, causing to be offered for sale, selling, causing to be sold, importing, and/or causing to be imported products that infringe one or more claims of the '984 Patent in this judicial district and elsewhere in the United States.

80. The products that are used, caused to be used, sold, caused to be sold, offered for sale, caused to be offered for sale, imported, and/or caused to be imported by

AUO, CMO, and CMO USA meet each and every limitation of at least one claim of the '984 Patent, either literally or equivalently.

81. LPL has been and will continue to be injured by AUO's, CMO's, and CMO USA's past and continuing infringement of the '984 Patent and is without adequate remedy at law.

82. AUO, CMO, and CMO USA, upon information and belief, infringed and is infringing the '984 Patent with knowledge of LPL's patent rights and without a reasonable basis for believing its conduct is lawful. AUO's, CMO's, and CMO USA's infringement has been and continues to be willful and deliberate, and will continue unless enjoined by this Court, making this an exceptional case and entitling LPL to increased damages and reasonable attorneys' fees pursuant to 35 U.S.C. §§ 284 and 285.

COUNTERCLAIM COUNT VIII
INFRINGEMENT OF THE '374 PATENT

83. LPL hereby incorporates paragraphs 58-82 above as though fully set forth herein.

84. AUO, CMO, and CMO USA have infringed, and/or induced infringement of the '374 Patent by making, using, causing to be used, offering to sell, causing to be offered for sale, selling, causing to be sold, importing, and/or causing to be imported products that infringe one or more claims of the '374 Patent in this judicial district and elsewhere in the United States.

85. The products that are used, caused to be used, sold, caused to be sold, offered for sale, caused to be offered for sale, imported, and/or caused to be imported by AUO, CMO, and CMO USA meet each and every limitation of at least one claim of the '374 Patent, either literally or equivalently.

86. LPL has been and will continue to be injured by AUO's, CMO's, and CMO USA's past and continuing infringement of the '374 Patent and is without adequate remedy at law.

87. AUO, CMO, and CMO USA, upon information and belief, infringed and is infringing the '374 Patent with knowledge of LPL's patent rights and without a reasonable basis for believing its conduct is lawful. AUO's, CMO's, and CMO USA's infringement has been and continues to be willful and deliberate, and will continue unless enjoined by this Court, making this an exceptional case and entitling LPL to increased damages and reasonable attorneys' fees pursuant to 35 U.S.C. §§ 284 and 285.

COUNTERCLAIM COUNT IX
CLAIM FOR DECLARATORY JUDGMENT OF INVALIDITY OF THE '944 PATENT, THE '157 PATENT, AND THE '506 PATENT AGAINST PLAINTIFF AU OPTRONICS CORPORATION

88. LPL hereby incorporates paragraphs 58-87 above as though fully set forth herein.

89. AUO has accused LPL of infringing the AUO Patents by filing counterclaims in this action. As such, there is a substantial controversy between the parties having adverse legal interests.

90. Claims of the '944 Patent are invalid for failure to satisfy one or more of the requirements for patentability set forth in Title 35 of the United States Code.

91. Claims of the '157 Patent are invalid for failure to satisfy one or more of the requirements for patentability set forth in Title 35 of the United States Code.

92. Claims of the '506 Patent are invalid for failure to satisfy one or more of the requirements for patentability set forth in Title 35 of the United States Code.

93. Because AUO has asserted the AUO Patents against LPL, thereby creating an actual controversy, declaratory relief is both appropriate and necessary to establish that one or more of the claims of the '944 Patent, the '157 Patent, and the '506 Patent are invalid.

COUNTERCLAIM COUNT X
CLAIM FOR DECLARATORY JUDGMENT OF NON-INFRINGEMENT OF THE '944 PATENT, THE '157 PATENT, AND THE '506 PATENT AGAINST PLAINTIFF AU OPTRONICS CORPORATION

94. LPL hereby incorporates paragraphs 58-93 above as though fully set forth herein.

95. LPL's LCD modules do not infringe any claim of the '944 Patent, either literally or under the doctrine of equivalents.

96. LPL's LCD modules do not infringe any claim of the '157 Patent, either literally or under the doctrine of equivalents.

97. LPL's LCD modules do not infringe any claim of the '506 Patent, either literally or under the doctrine of equivalents.

98. Because AUO maintains that LPL infringes the AUO Patents, thereby creating an actual controversy, a declaration of rights between LPL and AUO is both appropriate and necessary to establish that LPL has not infringed and does not infringe any claim of the '944 Patent, the '157 Patent, or the '506 Patent.

COUNTERCLAIM COUNT XI
CLAIM FOR DECLARATORY JUDGMENT OF UNENFORCEABILITY OF THE '944 PATENT AGAINST PLAINTIFF AU OPTRONICS CORPORATION

99. LPL hereby incorporates paragraphs 58-98 above as though fully set forth herein.

100. The '944 Patent relates to a liquid-crystal display having a photosensitive resin regulating cell gaps having dynamic hardness or plastic deformation values within a fixed range.

101. The listed inventors Toshihiko Koseki, Hidefumi Yamashita, Taro Hasumi, Yuichi Momoi, Yoshinori Shohmitsu, and Tomohito Johnai ("the Inventors") and the original assignee of the patent International Business Machines, Corp. ("IBM") knew of prior art references disclosing a photosensitive resin regulating cell gaps having a dynamic hardness value and a plastic deformation value within a fixed range that is the same as or similar to the claimed photosensitive resin of the '944 Patent, and on information and belief, willfully and with the intent to deceive the United States Patent and Trademark Office ("USPTO"), refrained from disclosing such references to the USPTO. Such prior art references include but are not limited to Japanese Patent ("JP") 06-273774, JP 05-080343, JP 03-287127, JP 04-191823, JP 06-265912, JP 62-090622, and JP 11-109372 (collectively, "the Japanese references").

102. On information and belief the Inventors and IBM knew of the teachings of the Japanese references before filing, or during the prosecution in the United States of application number 09/558,819 ("the US '819 application") for the '944 Patent. The Inventors and IBM filed patent application JP 11-122923 ("the JP '923 application") in Japan on April 28, 1999. This application to which the '944 Patent claims foreign priority is listed on the face of the '944 Patent. The JP '923 application discloses the same photosensitive resin for regulating cell gaps having a dynamic hardness value and a plastic deformation value within a fixed range as in the '944 Patent.

103. During the prosecution of the JP '923 application, the Examiner in the Japanese Patent Office issued a first Office Action on March 5, 2002, citing and discussing the Japanese references in rejecting the claims. The applicant amended the original claims in an attempt to overcome the Examiner's rejections. On April 16, 2003, the Japanese Patent Office Examiner issued an Advisory Action rejecting the amended claims, citing and discussing the same Japanese references. After learning of the Examiner rejections in the Office Action and Advisory Action in the Japanese priority application, the Inventors and assignee IBM continued to prosecute the co-pending US '819 application without disclosing these rejections to the USPTO. In fact, the Inventors and assignee IBM did not submit any Information Disclosure Statements during the prosecution of the '944 Patent application.

104. The applicant filed an Appeal in Japan from the Advisory Action on July 11, 2003, appealing the Examiner's rejections over the Japanese References. A Decision from the Japanese Patent Office on May 19, 2006 denied the Appeal on a number of grounds, including unpatentability over JP 06-273774, one of the Japanese references. As a result, the applicant abandoned the JP '923 application.

105. The Japanese references and their teachings were highly material to the patentability of the '944 Patent during its prosecution. On information and belief, the Japanese references would have been viewed as important by a reasonable Examiner. The Japanese references are not cumulative of other art of record in the US '819 application. The Japanese references alone or in combination with the other prior art references of record, would establish a prima facie case of unpatentability of one or more claims of the '944 Patent, and/or refute the arguments made by the applicant during the

prosecution of the US '819 application. On information and belief, the Inventors and assignee IBM knew, or should have known, the high materiality of the Japanese references.

106. On information and belief, the Inventors and IBM knew of material information relating to and arising from the Japanese Patent Office Examiner's rejections in the March 5, 2002 Office Action and the April 16, 2003 Advisory Action of the claims of the JP '923 application that are substantially similar to the issued claims of the '944 Patent, and willfully and with the intent to deceive the USPTO, refrained from disclosing such material information to the USPTO.

107. The original claim 1 of the JP '923 application, as filed on April 28, 1999, is the same or substantially similar to the claims of the '944 Patent as issued as original claim 1 of the JP '923 application contains a number of limitations that are the same or substantially similar to the limitations recited in the claims of the '944 Patent as issued.

108. An actual and justiciable controversy exists between the parties as to the enforceability of the '944 Patent. Declaratory relief is both appropriate and necessary to establish that the '944 Patent is unenforceable.

109. Because the Inventors and/or IBM failed to disclose material prior art and/or material information to the USPTO with the intent to deceive the USPTO during the prosecution of the '944 Patent, the '944 Patent is unenforceable due to inequitable conduct. LPL is entitled to a judicial declaration that the '944 Patent is unenforceable.

PRAYER FOR RELIEF

WHEREFORE, LPL prays for judgment as follows:

A. That the Court dismiss AUO's Counterclaims with prejudice;

B. That the '569 Patent, the '984 Patent, and the '374 Patent are valid and enforceable;

C. That AUO has infringed the '569 Patent, the '984 Patent, and the '374 Patent;

D. That AUO's infringement of the '569 Patent, the '984 Patent, and the '374 Patent has been willful;

E. That AUO and its parents, subsidiaries, affiliates, successors, predecessors, assigns, and the officers, directors, agents, servants and employees of each of the foregoing, and those persons acting in concert or participation with any of them, are enjoined and restrained from continued infringement, including but not limited to using, making, importing, offering for sale and/or selling products that infringe, and from inducing the infringement of, the '569 Patent, the '984 Patent, and the '374 Patent, prior to their expiration, including any extensions;

F. That AUO, its parents, subsidiaries, affiliates, successors, predecessors, assigns, and the officers, directors, agents, servants and employees of each of the foregoing, and those persons acting in concert or participation with any of them deliver to LPL all products that infringe the '569 Patent, the '984 Patent, and the '374 Patent for destruction at LPL's option;

G. That LPL be awarded monetary relief adequate to compensate LPL for AUO's acts of infringement of the '569 Patent, the '984 Patent, and the '374 Patent within the United States prior to the expiration of the '569 Patent, the '984 Patent, and the '374 Patent, including any extensions;

H. That any monetary relief awarded to LPL regarding the infringement of the '569 Patent, the '984 Patent, and the '374 Patent by AUO be trebled due to the willful nature of AUO's infringement of the '569 Patent, the '984 Patent, and the '374 Patent;

I. That CMO and CMO USA have infringed the '984 Patent and the '374 Patent;

J. That CMO's and CMO USA's infringement of the '984 Patent and the '374 Patent has been willful;

K. That CMO and CMO USA and their parents, subsidiaries, affiliates, successors, predecessors, assigns, and the officers, directors, agents, servants and employees of each of the foregoing, and those persons acting in concert or participation with any of them, are enjoined and restrained from continued infringement, including but not limited to using, making, importing, offering for sale and/or selling products that infringe, and from inducing the infringement of, the '984 Patent and the '374 Patent, prior to their expiration, including any extensions;

L. That CMO, CMO USA, their parents, subsidiaries, affiliates, successors, predecessors, assigns, and the officers, directors, agents, servants and employees of each of the foregoing, and those persons acting in concert or participation with any of them deliver to LPL all products that infringe the '984 Patent and the '374 Patent for destruction at LPL's option;

M. That LPL be awarded monetary relief adequate to compensate LPL for CMO's and CMO USA's acts of infringement of the '984 Patent and the '374 Patent within the United States prior to the expiration of the '984 Patent and the '374 Patent, including any extensions;

N. That any monetary relief awarded to LPL regarding the infringement of the '984 Patent and the '374 Patent by CMO and CMO USA be trebled due to the willful nature of CMO's and CMO USA's infringement of the '984 Patent and the '374 Patent;

O. That any monetary relief awarded to LPL be awarded with prejudgment interest;

P. That a post trial accounting be done as part of the monetary relief awarded to LPL;

Q. That the Court issue a declaratory judgment that LPL does not directly or indirectly infringe any Asserted AUO Patent under any applicable provision of 35 U.S.C. § 271;

R. That the Court issue a declaratory judgment that the Asserted AUO Patents are invalid;

S. That the Court issue a declaratory judgment that the '944 Patent is unenforceable;

T. That this is an exceptional case under 35 U.S.C. § 285 and that LPL be awarded the attorneys' fees, costs and expenses that it incurs prosecuting this action; and

U. That the Court award LPL other relief as it may find appropriate.

DEMAND FOR JURY TRIAL

Pursuant to Rule 38(b) of the Federal Rules of Civil Procedure, LG.Philips LCD Co., Ltd. respectfully demands a trial by jury on all issues so triable in this action.

August 8, 2007

THE BAYARD FIRM

/s/ Richard D. Kirk (rk0922)
Richard D. Kirk
Ashley B. Stitzer
222 Delaware Avenue, Suite 900
P.O. Box 25130
Wilmington, DE 19899
(302) 655-5000
Attorneys for Defendant/Counterclaim-Plaintiff LG.Philips LCD Co., Ltd.

OF COUNSEL:

Gaspare J. Bono
R. Tyler Goodwyn
Lora A. Brzezynski
McKenna Long & Aldridge LLP
1900 K Street, NW
Washington, D.C. 20006
(202) 496-7500

CERTIFICATE OF SERVICE

The undersigned counsel certifies that, on August 8, 2007, he served the foregoing documents by email and by hand upon the following counsel:

Edmond D. Johnson
Thomas H. Kovach
PEPPER HAMILTON LLP
1313 Market Street, Suite 5100
PO Box 1709
Wilmington, DE 19899-1709

Karen L. Pascale
John W. Shaw
YOUNG CONAWAY STARGATT & TAYLOR, LLP
The Brandywine Building
1000 West Street, 17th Floor
P.O. Box 391
Wilmington, DE 19899-0391

Philip A. Rovner
Dave E. Moore
POTTER ANDERSON & CORROON LLP
1313 North Market Street
Wilmington, DE 19899-0951

William E. Manning
Jennifer M. Becnel-Guzzo
BUCHANAN INGERSOLL & ROONEY
The Brandywine Building
1000 West Street, Suite 1410
Wilmington, DE 19801

The undersigned counsel further certifies that, on August 8, 2007, he served the foregoing documents by email and by U.S. Mail upon the following counsel:

John N. Zarian
Samia McCall
Matthew D. Thayne
STOEL RIVES LLP
101 S. Capitol Blvd., Suite 1900
Boise, ID 83702

Vincent K. Yip
Peter J. Wied
Jay C. Chiu
PAUL, HASTINGS, JANOFSKY & WALKER LLP
515 South Flower Street
Twenty-Fifth Floor
Los Angeles, CA 90071

Kenneth R. Adamo
Robert C. Kahrl
Arthur P. Licygiewicz
JONES DAY
North Point
901 Lakeside Avenue
Cleveland, OH 44114-1190

Bryan J. Sinclair
Karineh Khachatourian
BUCHANAN INGERSOLL & ROONEY
333 Twin Dolphin Drive, Suite 700
Redwood Shores, CA 94065-1418

Ron E. Shulman, Esquire
Julie Holloway, Esquire
WILSON SONSINI GOODRICH & ROSATI
650 Page Mill Road
Palo Alto, California 94304-1050

M. Craig Tyler, Esquire
Brian D. Range, Esquire
WILSON SONSINI GOODRICH & ROSATI
8911 Capital of Texas Highway North
Westech 360, Suite 3350
Austin, Texas 78759-8497

James R. Troupis, Esquire
Paul D. Barbato, Esquire
MICHAEL BEST & FRIEDRICH LLP
One South Pinckney Street
Suite 700
P.O.Box 1806
Madison, WI 53701-1806

/s/ Richard D. Kirk, (rk0922)
Richard D. Kirk

EXHIBIT A

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(12) **United States Patent**
Moon

(10) **Patent No.: US 6,664,569 B2**
(45) **Date of Patent: Dec. 16, 2003**

(54) **LIQUID CRYSTAL DISPLAY DEVICE ARRAY SUBSTRATE AND METHOD OF MANUFACTURING THE SAME**

(75) Inventor: **Hong-Man Moon**, Kumi-shi (KR)

(73) Assignee: **LG. Philips LCD Co., Ltd.**, Seoul (KR)

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(30) **Foreign Application Priority Data**

Jun. 9, 2000 (KR) 2000-31848

(51) **Int. Cl.**[7] **H01L 29/04**

(52) **U.S. Cl.** **257/72**; 257/59; 257/249; 257/401

(58) **Field of Search** 257/72, 59, 249, 257/245, 225, 401, 459, 331; 349/42

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Primary Examiner—Nathan J. Flynn
Assistant Examiner—Ahmed J. Sefer
(74) *Attorney, Agent, or Firm*—McKenna Long & Aldridge LLP

(57) **ABSTRACT**

An array substrate for use in a liquid crystal display device includes a thin film transistor as a switching element, having a gate electrode, a source electrode and a drain electrode, wherein the gate electrode is a portion of a gate line near the crossing of the gate and data lines, and has an inverted "T"-shaped opening or a rectangularly-shaped opening. The drain electrode is shaped like the inverted "T"-shape and corresponds to the opening of the gate electrode. The source electrode surrounds the drain electrode along the steps of the semiconductor layer. Accordingly, in the thin film transistor having this structure, the gate electrode is only overlapped by the edges of the drain electrode. And thus, the gate-drain parasitic capacitance is reduced and minimized. Also, variations in the gate-drain parasitic capacitance are prevented. As a result, a high resolution is achieved and the picture quality is improved in the liquid crystal display device.

37 Claims, 8 Drawing Sheets

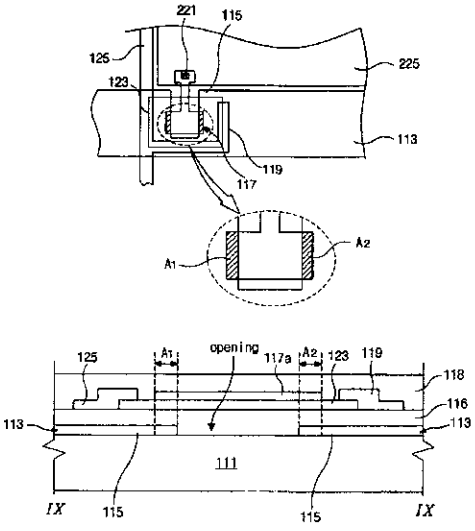


FIG.1
(RELATED ART)

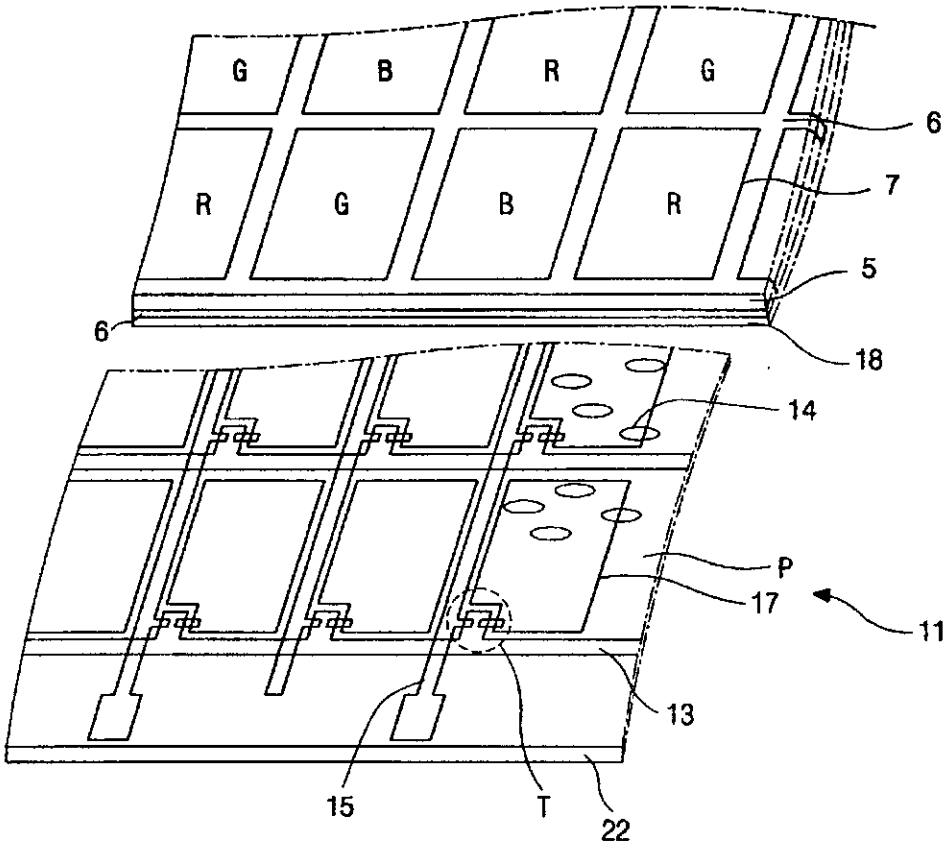


FIG.2
(RELATED ART)

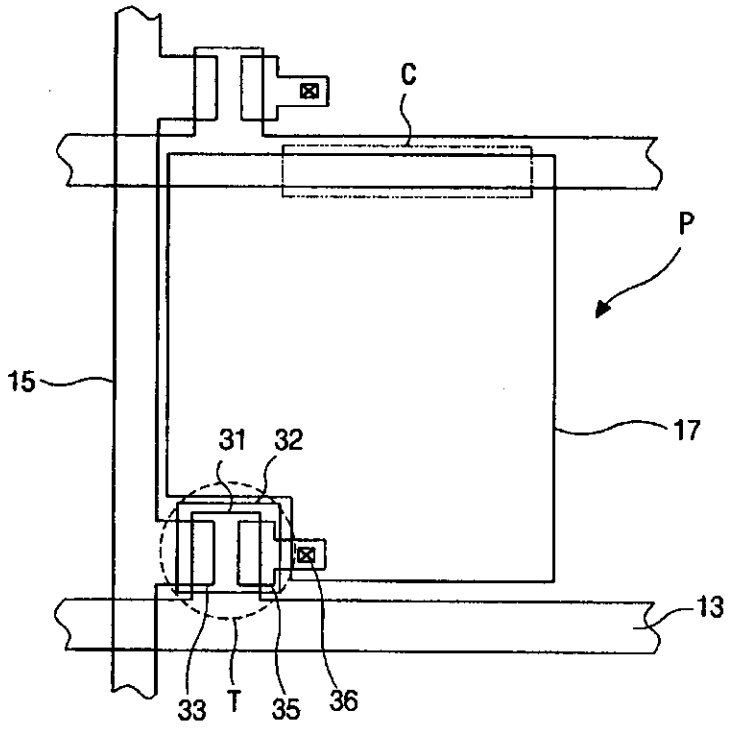


FIG.3
(RELATED ART)

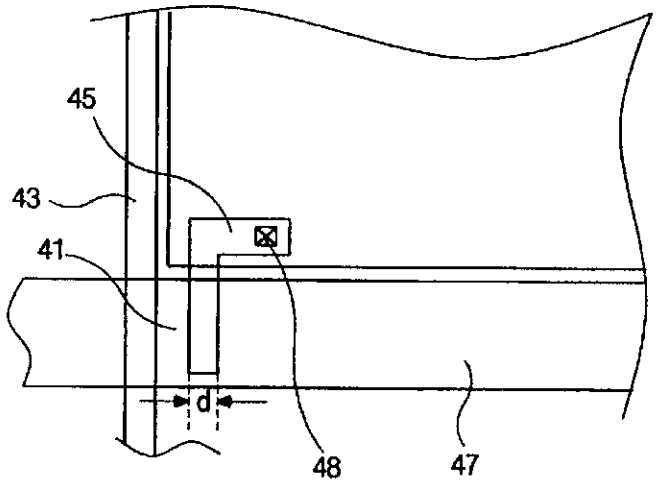


FIG.4
(RELATED ART)

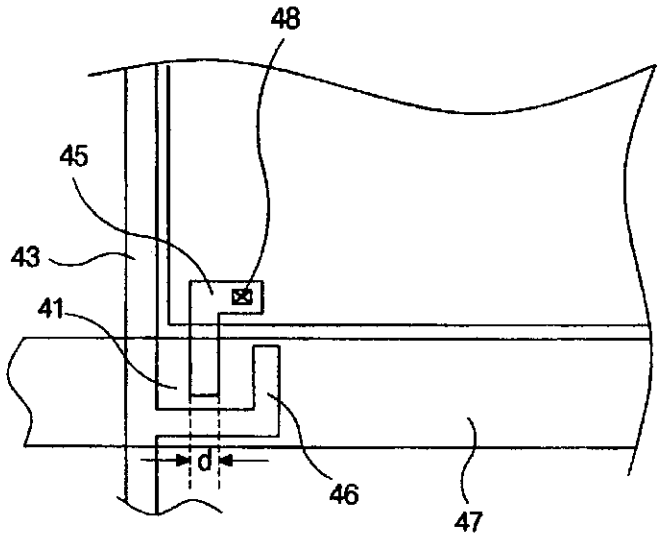


FIG.5

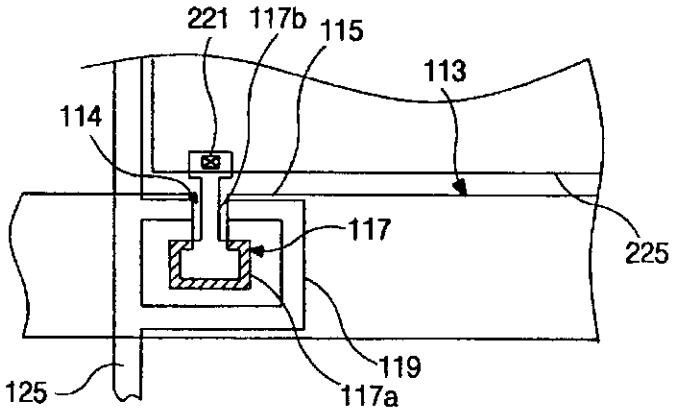


FIG.6A

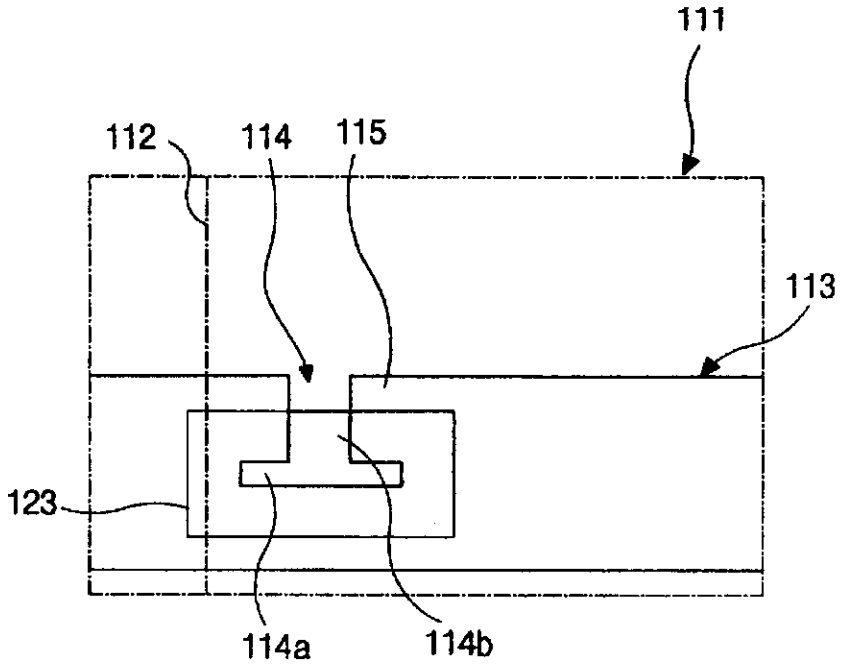


FIG.6B

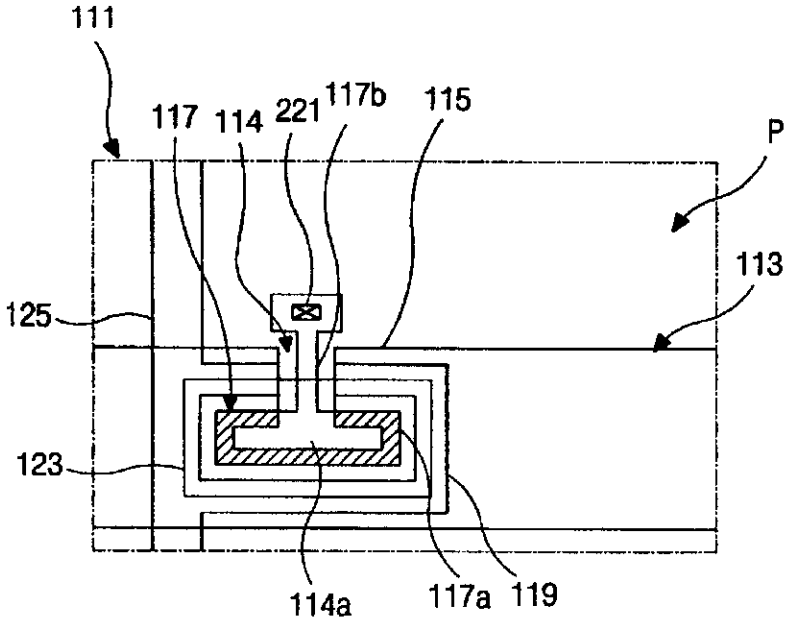


FIG.6C

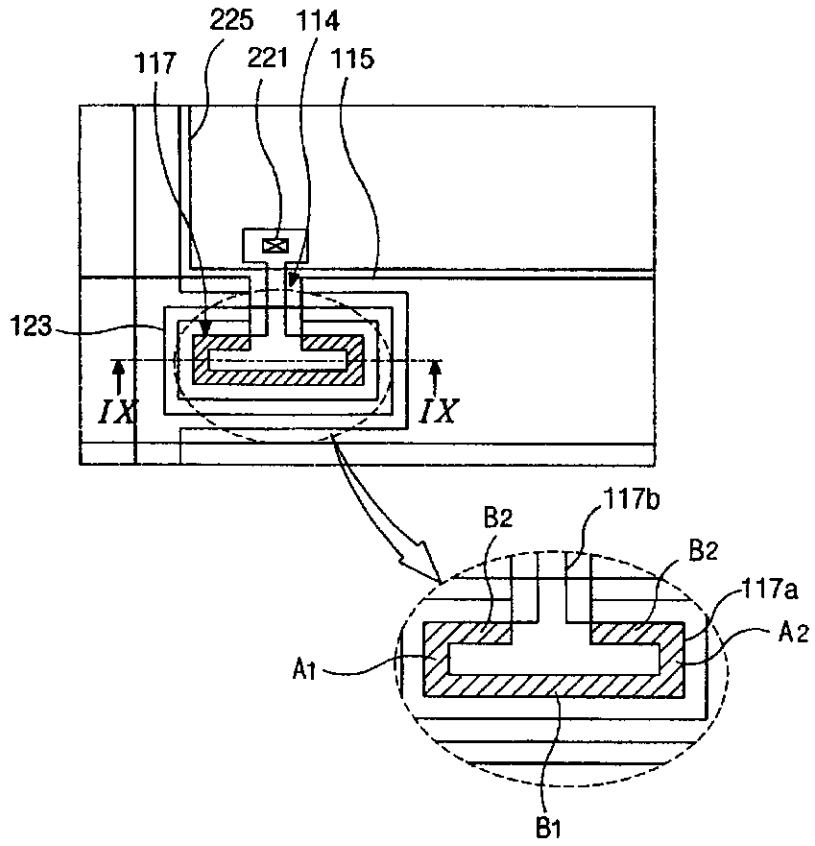


FIG.7

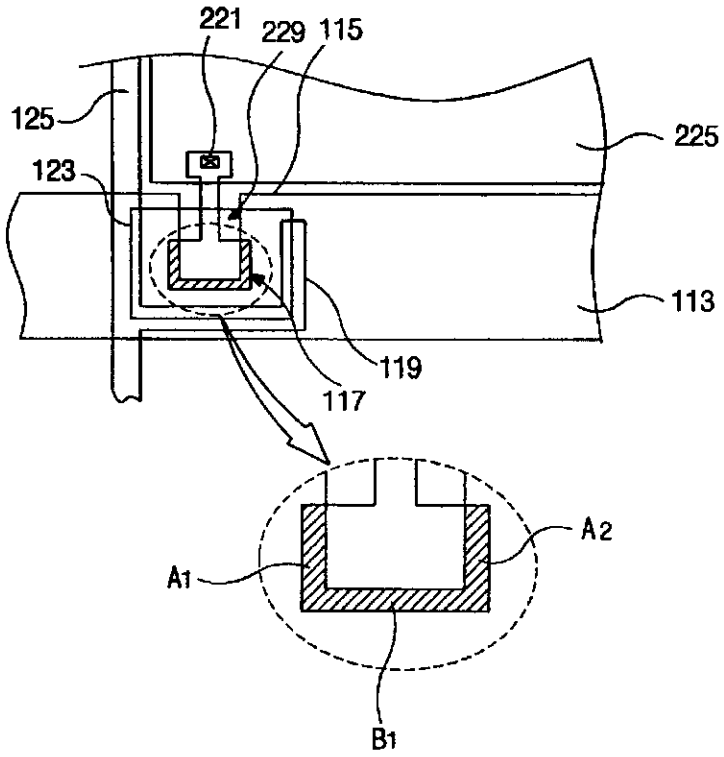


FIG.8

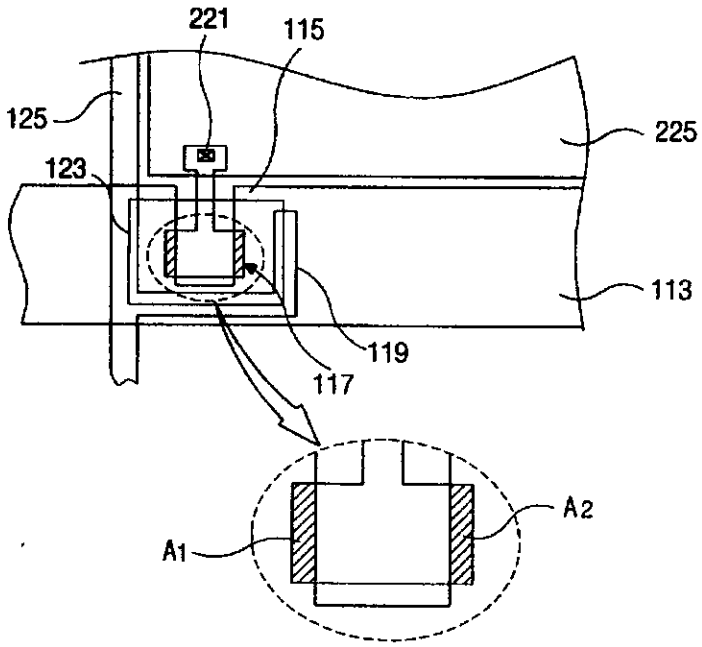
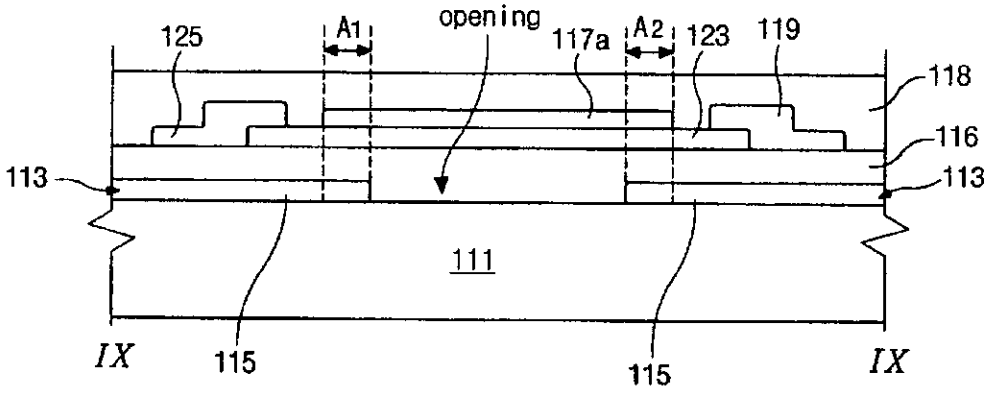

221
115
125
225
123
113
119
117
A2
A1

FIG.9


125
A1
opening
117a
A2
123
119
118
116
113
113
111
IX
115
115
IX

LIQUID CRYSTAL DISPLAY DEVICE ARRAY SUBSTRATE AND METHOD OF MANUFACTURING THE SAME

This application claims the benefit of Korean Patent Application No. 2000-31848, filed on Jun. 9, 2000, the entirety of which is hereby incorporated by reference for all purposes as if fully set forth herein.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to an array substrate for use in a liquid crystal display (LCD) device, and more particularly, an array substrate having a thin film transistor (TFT) with a reduced parasitic capacitance.

2. Discussion of the Related Art

FIG. **1** shows the configuration of a typical TFT-LCD device. The TFT-LCD device **11** includes upper and lower substrates **5** and **22** with an interposed liquid crystal material **14**. The upper and lower substrates **5** and **22** are generally referred to as a color filter substrate and an array substrate, respectively.

On the upper substrate **5**, on a surface opposing the lower substrate **22**, black matrix **6** and color filter layer **7**, including a plurality of red (R), green (G), and blue (B) color filters, are formed in the shape of an array matrix, such that each color filter is surrounded by the black matrix **6**. Also, on the upper substrate **5** a common electrode **18** is formed covering the color filter layer **7** and the black matrix **6**.

On the lower substrate **22**, on a surface opposing the upper substrate **5**, a thin film transistor (TFT) "T", as a switching device, is formed in the shape of an array matrix corresponding to the color filter layer **7**, and a plurality of crossing gate and data lines **13** and **15** are positioned such that each TFT "T" is located near each crossover point of the gate and data lines **13** and **15**. Also, on the lower substrate **22** a plurality of pixel electrodes **17** are formed in an area defined by the gate and data lines **13** and **15**. The area defined thereby is a pixel region "P". The pixel electrode **17** is usually formed from a transparent conductive material having good transmissivity, for example, indium-tin-oxide (ITO) or indium-zinc-oxide (IZO).

The pixel and common electrodes **17** and **18** generate electric fields that control the light passing through the liquid crystal cells provided therebetween. By controlling the electric fields, desired characters or images are displayed.

The operation of the TFT-LCD device having the above-mentioned structure is based on the a principle that the alignment direction of the liquid crystal molecules depends on an applied electric field. Namely, the liquid crystal layer having a spontaneous polarization characteristic is a dielectric anisotropy material. The liquid crystal molecules have dipole moments based on the spontaneous polarization when a voltage is applied. Thus, the alignment direction of the liquid crystal molecules is controlled by applying an electric field to the liquid crystal molecules. When the alignment direction of the liquid crystal molecules is properly adjusted, the liquid crystals are aligned and light is refracted along the alignment direction of the liquid crystal molecules to display image data. The liquid crystal molecules function as an optical modulation element having optical characteristics that vary depending upon the polarity of the applied voltage.

FIG. **2** is a plan view illustrating one pixel of an array substrate for the liquid crystal display device according to a related art. As shown, the array substrate includes gate line

13 arranged in a transverse direction; data line **15** arranged in a longitudinal direction perpendicular to the gate line **13**; and a thin film transistor (TFT) "T" as a switching element formed near the crossing of the gate and data lines **13** and **15**. The TFT "T" has a gate electrode **31**, a source electrode **33** and a drain electrode **35**. The gate electrode **31** is extended from the gate line **13**, and the source electrode **33** is extended from the data line **15**. The drain electrode **35** is spaced apart from the source electrode **33**. The source and drain electrodes **33** and **35** respectively overlap both ends of the gate electrode **31**. The TFT "T" also has a semiconductor layer **32** that is made of amorphous silicon (a—Si:H) or poly-silicon.

Moreover, the array substrate further includes a pixel electrode **17** formed on a pixel region "P" that is defined by the gate and data lines **13** and **15**. The pixel electrode **17** is electrically connected with the drain electrode **35** through a drain contact hole **36**, and is usually made of a transparent conductive material such as indium tin oxide (ITO) and indium zinc oxide (IZO). A portion of the pixel electrode **17** overlaps a portion of the gate line **13** such that a storage capacitor "C" is comprised of the pixel electrode **17** and gate line **13** and the interposed dielectric layer (not show).

Still referring to FIG. **2**, the gate line **13** supplies scanning signals to the gate electrode **31** of the TFT "T" such that the switching element, i.e., the TFT, turns ON. The scanning signals transmitted to the gate line **13** then control the magnitude of the data signals transmitted from the data line **15** to the pixel electrode **17** via the TFT "T." The data signals of the pixel electrode **17** cause the polarization and re-arrangement of the liquid crystal molecules that are disposed over the pixel electrode **17**. When the scanning signals are not supplied to the gate line **13**, the TFT "T" is turned OFF. At this time, electric charges stored in the pixel are discharged through the TFT "T" and through the liquid crystals. In this discharge phenomenon, if the off resistance is larger or if the pixel area is smaller for improving the resolution, the electric charges stored in the pixel are more rapidly discharged.

In order to solve these problems, the storage capacitor "C" has a parallel connection with the pixel electrode **17** and compensates for electric discharges. Thus, the data signal is maintained in the pixel. At this time, the data signal, however, is affected by source-gate or drain-gate parasitic capacitance. This effect leads to pixel flickering, image retention and non-uniform display.

In general, the parasitic capacitance occurs between the source and gate electrodes **33** and **31** of the TFT "T" or between the drain and gate electrodes **35** and **31** of the TFT "T". The parasitic capacitance between the source and gate electrodes **33** and **31** is referred to as source-gate or gate-source parasitic capacitance (C_{gs} or C_{sg}). The parasitic capacitance between the drain and gate electrodes **35** and **31** is referred to as drain-gate or gate-drain parasitic capacitance (C_{dg} or C_{gd}). When the semiconductor layer **32** is fully saturated by the electric charges, the gate-drain parasitic capacitance C_{gd} is increased due to the fact that the electric charges stored in the pixel electrode **17** are transmitted to the drain electrode **35**. Again, this parasitic capacitance causes pixel flickering, the image retention, and gray scale nonuniformity. Thus, it is essentially required to decrease the gate-drain parasitic capacitance C_{gd}.

Still referring to FIG. **2**, the gate electrode **31** is protruded from the gate line **13** over the pixel region "P" near the crossing of the gate and data lines **13** and **15**. The source and drain electrodes **33** and **35** overlap both ends of the gate electrode **31**. In this structure shown in FIG. **2**, the gate-drain

parasitic capacitance C_{gd} is defined by an area in which the drain electrode **35** overlaps the gate electrode **31**. Moreover, misalignment often occurs between the gate and drain electrodes **31** and **35** when forming the co-planar source and drain electrodes **33** and **35** over both ends of the gate electrode **31** using a pattern process. Thus, the gate-drain parasitic capacitance C_{gd} varies owing to this misalignment between the gate and drain electrodes **31** and **35**. For example, if the width and length of the drain electrode **35** are respectively 30 μm and 5 μm, the ratio of the width and the length is 30 to 5. In this case, the overlapped ratio of the drain electrode **35** is usually determined to be 30 to 4, and thus the overlapped area between the drain and gate electrodes becomes 120 μm^2 (i.e., 30 μm×4 μm). However, if the drain electrode **35** horizontally further overlaps by 1 μm, the overlapped area between the gate and drain electrodes **31** and **35** is 150 μm^2 (i.e., 30 μm×5 μm). Further, if the drain electrode **35** horizontally less overlaps by 1 μm, the overlapped area between the gate and drain electrodes **31** and **35** is 90 μm^2. These means that a misalignment of 1 μm causes great variations of the gate-drain parasitic capacitance C_{gd} by 25%.

As described above, the parasitic capacitance fluctuates depending on the overlapped area, and the unstable parasitic capacitance affects the data signal transmitted from the data line to the pixel electrode through the TFT. Accordingly, the display characteristics of the liquid crystal display become irregular. As a result, the picture quality is deteriorated by these irregular display characteristics.

FIGS. **3** and **4** are schematic partial plan views illustrating the crossover point of the gate and data lines of an array substrate for the liquid crystal display device according to another related art. As shown, in contrast to the above-mentioned array substrate, a gate electrode **41** is formed in the gate line **47**. Namely, a portion of the gate line **47**, near the crossing of the gate and data lines **47** and **43**, is used as the gate electrode **41**. In order to form the TFT, a drain electrode **45** is formed over the gate line **47**. Thus, the gate-drain parasitic capacitance C_{gd} is determined by an area of the drain electrode **45**.

Referring to FIG. **3**, a portion of the data line **43**, in which the gate line **47** is overlapped, functions as a source electrode. However, although FIG. **4** is similar to FIG. **3**, a source electrode **46** of FIG. **4** is extended from the gate line **43** over the gate line **47**. As shown in FIG. **4**, the source electrode **46** has a U-shape in order to increase the width of the channel region between the drain electrode **45** and the source electrode **46**. Even though the structure of the drain electrode **45** causes parasitic capacitance, as shown in FIGS. **3** and **4**, the variation of the parasitic capacitance that is caused by the misalignment is smaller than the above-mentioned TFT depicted in FIG. **2**. However, whenever the drain electrode pattern becomes smaller and smaller in order to lower the parasitic capacitance, the process control for forming the drain electrode is difficult and at least an error of about 1 μm surely occurs in the overlapped area. And thus, a critical dimension loss occurs during the patterning process.

In order to overcome the above-mentioned problem, the drain electrode **45** is designed to have a sufficiently large dimension. Thus, the horizontal length "d" is enlarged. At this time, the gate-drain parasitic capacitance C_{gd}, however, is also enlarged.

Accordingly, as described before, due to not only the gate-drain parasitic capacitance but also the variation of that parasitic capacitance, the pixel flickering and other image deteriorations occur in the liquid crystal display device.

SUMMARY OF THE INVENTION

Accordingly, the present invention is directed to an array substrate of a liquid crystal display device that substantially obviates one or more of the problems due to limitations and disadvantages of the related art.

To overcome the problems described above, the present invention provides an array substrate that has a novel structure for decreasing the gate-drain parasitic capacitance.

Another object of the invention is to provide an array substrate that decreases an overlapped area between gate and drain electrodes.

Additional features and advantages of the invention will be set forth in the description which follows, and in part will be apparent from the description, or may be learned by practice of the invention. The objectives and other advantages of the invention will be realized and attained by the structure particularly pointed out in the written description and claims thereof as well as the appended drawings.

To achieve these and other objects and in accordance with the purpose of the present invention, as embodied and broadly described, an array substrate for use in a liquid crystal display device having a lower gate-drain parasitic capacitance includes a gate line arranged in a horizontal direction on a substrate; a data line arranged in a vertical direction perpendicular to the gate line over the substrate; and a thin film transistor formed near the crossing of the gate and data lines, the thin film transistor comprising a gate electrode that is a portion of the gate line near the crossing, wherein the gate electrode has an open portion in its central portion, a first insulation layer on the gate electrode, a semiconductor layer formed on the first insulation layer and over the gate electrode, a drain electrode formed on the semiconductor layer and over the gate electrode, the drain electrode corresponding to the open portion of the gate electrode, and a source electrode extended from the data line and formed in the same plane as the drain electrode, the source electrode surrounding the drain electrode and the open portion of the gate electrode along the steps of the semiconductor layer.

The array substrate further includes a second insulation layer formed over the thin film transistor, the second insulation layer having a drain contact hole that exposes a portion of the drain electrode; and a pixel electrode formed in a pixel region that is defined by the gate and data lines, the pixel electrode contacting the drain electrode through the drain contact hole.

In one embodiment, the open portion of the gate electrode has an inverted "T"-shape and first and second open portions. The first open portion is formed in a horizontal direction parallel with the gate line and the second open portion is formed in a vertical direction perpendicular to the first open portion. The drain electrode also has an inverted "T"-shape and includes first and second electrode portions. The first electrode portion is arranged in a horizontal direction parallel with the gate line and corresponds to the first open portion of the gate electrode. And the second electrode portion is arranged in a vertical direction perpendicular to the first electrode portion and corresponds to the second open portion.

The open portion of the gate electrode can also be shaped like a rectangle.

Edges of the first electrode portion of the drain electrode overlap the gate electrode. Namely, two or three side edges of the first electrode portion overlap the gate electrode.

It is to be understood that both the foregoing general description and the following detailed description are exem-

plary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWING

The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and together with the description serve to explain the principles of the invention.

In the drawings:

FIG. **1** shows the configuration of a typical TFT-LCD device;

FIG. **2** is a plan view illustrating one pixel of an array substrate for the liquid crystal display device according to a related art;

FIGS. **3** and **4** are schematic partial plan views illustrating the crossover point of the gate and data lines of an array substrate for the liquid crystal display device according to related arts;

FIG. **5** is a schematic partial view illustrating the crossover point of the gate and data lines of an array substrate according to a first embodiment;

FIGS. **6**A to **6**C are plan views illustrating a manufacturing process for the array substrate of FIG. **5**;

FIG. **7** is a schematic partial plan view illustrating the crossover point of the gate and data lines of an array substrate according to a second embodiment;

FIG. **8** is a schematic partial plan view illustrating the crossover point of the gate and data lines of an array substrate according to a third embodiment; and

FIG. **9** is a cross-sectional view taken along line IX—IX of FIG. **6**C and illustrates layer elements of the thin film transistor according to a principle of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Reference will now be made in detail to embodiments of the present invention, which are illustrated in the accompanying drawings.

FIG. **5** is a schematic partial plan view illustrating the crossover point of gate and data lines of an array substrate according to a first embodiment. As shown, the array substrate includes a gate line **113**, which is arranged in a horizontal direction, and a data line **125**, which is arranged in a vertical direction. The gate line **113** has a portion used for a gate electrode **115** near the crossing of the gate and data lines **113** and **125**. In the central portion of the gate line **113** used for gate electrode **115**, an inverted "T"-shaped opening **114** is formed. The source electrode **119** is extended from the data line **125**, and has a quadrilateral opening in its central portion. Thus, the source electrode **119** surrounds the inverted "T"-shaped opening in the gate line **113**. The drain electrode **117** is shaped like the inverted "T"-shape and positioned corresponding to the inverted "T"-shaped opening **114** of the gate electrode **115**. Moreover, the drain electrode **117** is divided into a first electrode portion **117***a* and a second electrode portion **117***b*. And thus, the source electrode **119** also surrounds the first electrode portion **117***a* of the drain electrode **117**. As shown in FIG. **5**, at the end of the second electrode portion **117***b* of the drain electrode **117**, a drain contact hole **221** is formed, thus a pixel electrode **225** is electrically connected with the drain electrode **117** through this drain contact hole **221**.

Still referring to FIG. **5**, in order to decrease an overlapped area between the gate electrode **115** and the drain electrode **117**, the portion of the gate electrode **115** under the drain electrode **117** is etched such that the inverted "T"-shaped opening **114** is formed. In other words, the portion of the gate electrode **115** corresponding to the first electrode portion **117***a* of the drain electrode **117** is etched in a smaller area than the first electrode portion **117***a*. Thus, edges of the first electrode portion **117***a* of the drain electrode **117** overlap the gate electrode **115**. Moreover, a portion of the gate electrode **115** under the second electrode portion **117***b* is etched in a wider area than the second electrode portion **117***b* of the drain electrode **117**. Thus, the gate electrode **115** is not overlapped by this second electrode portion **117***b*.

Accordingly, as described above, since the edges of the first electrode portion **117***a* of the drain electrode **117** only overlap the gate electrode **115**, the gate-drain parasitic capacitance that depends on the overlapped area is minimized.

FIGS. **6**A to **6**C are plan views illustrating a manufacturing process for the array substrate of FIG. **5**, and FIG. **9** is a cross-sectional view taken along line IX—IX of FIG. **6**C.

Referring to FIG. **6**A and FIG. **9**, a first metal layer is formed on a substrate **111** by depositing a metallic material selected from a group consisting of aluminum (Al), chrome (Cr), molybdenum (Mo), tungsten (W) and the like. After that, the first metal layer is patterned so as to form the gate line **113** in a horizontal direction, and an imaginary line **112** where the data line is formed in a later step is defined. At this time, near the crossover point of the gate line **113** and imaginary line **112**, a portion of the gate line **113** is etched so as to form the inverted "T"-shaped opening **114** and the gate electrode **115** is defined there around. The inverted "T"-shaped opening **114** is divided into a first opening portion **114***a* and a second opening portion **114***b*. The first opening portion **114***a* is horizontally disposed in parallel with the gate line **113** in the gate electrode **115**, and the second opening portion **114***b* is vertically elongated from a top edge to a center of the gate line **113** in the gate electrode **115**. Thereby, the gate electrode **115** includes the inverted "T"-shaped opening **114** having the first and second opening portion **114***a* and **114***b*.

Further, although not depicted in FIG. **6**A but shown in FIG. **9**, a first insulation layer **116** is formed on the substrate **111** and gate line **113** by depositing an inorganic material, such as silicon nitride (SiN_x) or silicon oxide (SiO_2), or an organic material, such as benzocyclobutene (BCB) or acryl.

Thereafter, an amorphous silicon layer and impurity-included-amorphous silicon layer are formed successively. The amorphous silicon layer and the impurity-included-amorphous silicon layer are patterned into an island-shaped layer so as to form a semiconductor layer **123**. As shown in FIG. **6**A, the semiconductor layer **123** is located over the inverted "T"-shaped opening **114** of the gate electrode **115** and is larger than the first opening portion **114***a*.

Referring to FIGS. **6**B and **9**, a second metal layer is formed on the entire surface of the substrate **111** including the gate line **113**, a first insulation layer **116** and the semiconductor layer **123**. The second metal layer is the same kind of material as the first metal layer. After that, the second metal layer is patterned so as to form the data line **125** in the area defined by the imaginary line **112** of FIG. **6**A. Thus, the data line **125** is perpendicular to the gate line **113** and, with the gate line **113** defines a pixel area "P." During this patterning process, the source electrode **119** extended from the data line **125** is simultaneously formed over the gate electrode **115**. The shape of the source electrode **119** is a quadrilateral and has a quadrilateral opening therein such

that the source electrode **119** surrounds the first opening portion **114***a* of the inverted "T"-shaped opening **114**. Also, the drain electrode **117** is simultaneously formed over the inverted "T"-shaped opening **114** in the same plane as the source electrode **119**.

Still referring to FIGS. **6**B and **9**, the drain electrode **117** is patterned into an inverted "T"-shape and corresponds to the inverted "T"-shaped opening **114** of the gate electrode **115**. Again, the drain electrode **117** is divided into the first electrode portion **117***a* and the second electrode portion **117***b*. The first electrode portion **117***a* overlaps the gate electrode **115** such that the edges of the first electrode portion **117***a* form a "U"-shaped overlapped area (depicted by oblique lines) with the gate electrode **115**. The second electrode portion **117***b* is vertically extended from the first electrode portion **117***a* over the pixel area "P," and does not overlaps the gate electrode **115** due to the fact that the second electrode portion **117***b* is narrower than the second opening portion **114***b* of FIG. **6**A. Moreover, the drain electrode **117** is spaced apart from the source electrode **119**, and the first electrode portion **117***a* of the drain electrode **117** is surrounded by the source electrode **119** along the steps of the semiconductor layer **123**.

Further, although not depicted in FIG. **6**B but depicted in FIG. **9**, a second insulation layer **118** is formed on the above-mentioned intermediates by depositing an inorganic material, such as silicon nitride (SiN_x) or silicon oxide (SiO_2), or an organic material, such as benzocyclobutene (BCB) or acryl. Next, the second insulation layer (not shown) is patterned in order to form a drain contact hole **221** at the end of the second electrode portion **117***b* of the drain electrode **117**.

Now, referring to FIG. **6**C, a transparent conductive material such as indium-tin-oxide (ITO) or indium-zinc-oxide (IZO) is deposited on the above-mentioned second insulation layer. After that, the transparent conductive material is patterned to form a pixel electrode **225** in the pixel region "P" (see FIG. **6**B). And thus, the pixel electrode **225** contacts the drain electrode **117** through the drain contact hole **221**.

As described hereinbefore, since only the edges of the fist electrode portion of the drain electrode overlaps the gate electrode, the gate-drain parasitic capacitance C_{gd} is reduced and minimized due to the smaller overlapped area. Moreover, referring to the enlarged view of the first electrode portion of the drain electrode as shown in FIG. **6**C, the compensation for any misalignment will be explained. When forming the drain electrode **117** over the inverted "T"-shaped opening **114** of the gate electrode **115**, the drain electrode **117** can be misaligned in a horizontal or vertical direction. If the left portion "A_1" of the overlapped area is decreased due to horizontal misalignment, the right portion "A_2" is increased. In this manner, if the bottom portion "B_1" of the overlapped area is decreased due to vertical misalignment, the top portion "B_2" is increased. Thus, the overlapped area between the drain electrode **117** and the gate electrode **115** is maintained uniformly even though misalignment occurs. Therefore, the variation of the gate-drain parasitic capacitance is reduced and minimized.

FIG. **7** is a schematic partial plan view illustrating the crossover point of the gate and data lines of an array substrate according to a second embodiment. As shown, the second embodiment is similar to the first embodiment depicted in FIG. **5** and the manufacturing process is the same as the first embodiment depicted in FIGS. **6**A to **6**C and in FIG. **9**. However, the gate line **113** has a rectangle-shaped opening **229** in a portion for the gate electrode **115**.

Referring to FIG. **7**, the source electrode **119** is extended from the data line and has a "U"-shape. The drain electrode **117** is formed into an inverted "T"-shape and located over the rectangle-shaped opening **229** of the gate electrode **115**. The drain electrode **117** is also surrounded by the source electrode **119** along the steps of the semiconductor layer **123**, as in the first embodiment. Moreover, edges of the drain electrode **117** overlap the gate electrode **115**, and thus the overlapped area is formed generally with a "U"-shape (depicted by oblique lines). As a result, the gate-drain parasitic capacitance C_{gd} is reduced and minimized as in the first embodiment.

Moreover, referring to the enlarged view of the drain electrode **117** of FIG. **7**, any misalignment occurring in the step of forming the drain electrode **117** is compensated. When forming the drain electrode **117** over the rectangle-shaped opening **229** of the gate electrode **115**, the drain electrode **117** can be misaligned in a horizontal or vertical direction. If the left portion "A_1" of the overlapped area is decreased due to horizontal misalignment, the right portion "A_2" is increased. In this manner, if the bottom portion "B_1" of the overlapped area is decreased due to vertical misalignment, the left and right portions "A_1" and "A_2" are increased. Thus, the overlapped area between the drain electrode **117** and the gate electrode **115** is maintained uniformly even though the misalignment occurs. Therefore, the variation of the gate-drain parasitic capacitance is lowered and minimized.

FIG. **8** is a schematic partial view illustrating the crossover point of the gate and data lines of an array substrate according to a third embodiment. As shown, the third embodiment is similar to the second embodiment and the manufacturing process is the same as the second embodiment. However, the overlapped area (depicted by oblique lines) is formed on both end sides of the drain electrode **117**.

As shown in FIG. **8**, the gate line **113** is arranged in a horizontal direction and the data line **125** is arranged in a vertical direction perpendicular to the gate line **113**. The source electrode **119** is extended from the data line **125** and has a "U"-shape. A rectangle-shaped opening is formed in a portion for the gate electrode **115** in the gate line **113**. Also, the drain electrode **117** is formed over the rectangle-shaped opening of the gate electrode **115**. Although the drain electrode **117** has an inverted "T"-shape, only both end sides of the drain electrode **117** overlap the gate electrode. Thus, the overlapped area (depicted in oblique lines) is reduced and minimized, and the gate-drain parasitic capacitance C_{gd} is also reduced and minimized.

Moreover, referring to the enlarged view of the drain electrode **117** as shown in FIG. **8**, any misalignment occurring in the step of forming the drain electrode **117** is compensated. When forming the drain electrode **117** over the rectangle-shaped open of the gate electrode **115**, the drain electrode **117** can be misaligned in a horizontal direction. If the left portion "A_1" of the overlapped area is decreased due to horizontal misalignment, the right portion "A_2" is increased. Thus, the overlapped area between the drain electrode **117** and the gate electrode **115** is maintained uniformly even though misalignment occurs. Therefore, the variation of the gate-drain parasitic capacitance is reduced and minimized.

As described hereinbefore, according to the principles of the present invention, a portion of the gate line is used as the gate electrode. And a portion of the gate electrode is patterned so as to form a certain-shaped opening. Accordingly, there is a reduced overlap area between the

gate electrode and the drain electrode. As a result, the gate-drain parasitic capacitance is reduced and minimized. Moreover, although misalignment occurs between the drain and gate electrodes, this misalignment is compensated according to the present invention. Thus, the variation of the gate-drain parasitic capacitance is prevented.

Therefore, flickering and the image retention are prevented so that a high resolution is achieved in the liquid crystal display device. And the picture quality is improved in the liquid crystal display device.

It will be apparent to those skilled in the art that various modifications and variation can be made in the present invention without departing from the spirit or scope of the invention. Thus, it is intended that the present invention cover the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.

What is claimed is:

1. An array substrate for use in a liquid crystal display device, comprising:

a gate line arranged in a horizontal direction on a substrate;

a data line arranged in a vertical direction perpendicular to the gate line over the substrate; and

a thin film transistor formed near a crossing of the gate and data lines, the thin film transistor comprising:

a gate electrode that is a portion of the gate line near said crossing, wherein the gate electrode has an opening portion in its central portion;

a first insulation layer on the gate electrode;

a semiconductor layer formed on the first insulation layer and over the gate electrode;

a drain electrode formed on the semiconductor layer and over the gate electrode, the drain electrode corresponding to the opening of the gate electrode; and

a source electrode extended from the data line and formed in a same plane as the drain electrode, the source electrode surrounding the drain electrode and opening of the gate electrode along steps of the semiconductor layer.

2. The array substrate according to claim **1**, further comprising a second insulation layer formed over the thin film transistor, the second insulation layer having a drain contact hole that exposes a portion of the drain electrode.

3. The array substrate according to claim **2**, further comprising a pixel electrode formed in a pixel region that is defined by the gate and data lines, the pixel electrode contacting the drain electrode through the drain contact hole.

4. The array substrate according to claim **1**, wherein the opening of the gate electrode has an inverted "T"-shape.

5. The array substrate according to claim **4**, wherein the opening of the gate electrode includes first and second opening portions.

6. The array substrate according to claim **5**, wherein the first opening portion is formed in a horizontal direction parallel with the gate line.

7. The array substrate according to claim **5**, wherein the second opening portion is formed in a vertical direction perpendicular to the first opening portion.

8. The array substrate according to claim **1**, wherein the drain electrode has an inverted "T"-shape.

9. The array substrate according to claim **8**, wherein the drain electrode includes first and second electrode portions.

10. The array substrate according to claim **9**, wherein the first electrode portion is arranged in a horizontal direction parallel with the gate line and corresponds to the first opening portion of the gate electrode.

11. The array substrate according to claim **9**, wherein the second electrode portion is arranged in a vertical direction perpendicular to the first electrode portion and corresponds to the second opening portion.

12. The array substrate according to claim **1**, wherein the opening of the gate electrode is shaped like a rectangle.

13. The array substrate according to claim **12**, wherein the drain electrode has an inverted "T"-shape and first and second electrode portions.

14. The array substrate according to claim **13**, wherein edges of the first electrode portion overlap the gate electrode.

15. The array substrate according to claim **14**, wherein three side edges of the first electrode portion overlap the gate electrode.

16. The array substrate according to claim **14**, wherein two side edges of the first electrode portion overlap the gate electrode.

17. A liquid crystal display (LCD) device, comprising:

a substrate;

a gate line on the substrate and extending along a first direction, the gate line having an opening therein;

a first insulating layer on the gate line;

a semiconductor layer on the first insulating layer over at least a portion of the opening;

a data line on the insulating layer and extending along a second direction substantially perpendicular to the first direction;

a drain electrode on the semiconductor layer over at least a portion of the opening; and

a source electrode on the semiconductor layer, extending from the data line and being separated and spaced apart from the drain electrode.

18. The LCD device of claim **17**, further comprising a second insulation layer over the semiconductor layer and the source and drain electrodes, the second insulation layer having a drain contact hole that exposes a portion of the drain electrode.

19. The LCD device to claim **18**, further comprising a pixel electrode disposed in a pixel region that is defined by an intersection of the gate and data lines, the pixel electrode contacting the drain electrode through the drain contact hole.

20. The LCD device of claim **17**, wherein the opening in the gate line has substantially a "T" shape.

21. The LCD device of claim **17**, wherein the source electrode substantially surrounds the drain electrode.

22. The LCD device of claim **17**, wherein the drain electrode has substantially a "T" shape.

23. The LCD device of claim **17**, wherein the drain electrode comprises:

a first portion which overlaps the opening; and

a second portion which overlaps the gate line on at least two opposing sides of the opening.

24. The liquid crystal display (LCD) device of claim **17**, wherein the source electrode surrounds the drain electrode and the opening of the gate electrode along steps of the semiconductor layer.

25. A liquid crystal display (LCD) device, comprising:

a substrate;

a gate line on the substrate and extending along a first direction, the gate line including a gate electrode, the gate electrode having an opening therein, wherein the opening includes a first opening portion and a second opening portion;

a first insulating layer on the gate line;

a semiconductor layer on the first insulating layer;

a data line on the insulating layer and extending along a second direction;

a drain electrode having a first electrode and a second electrode, the first electrode of the drain electrode overlapping at least a part of the first opening portion of the gate electrode; and

a source electrode on the semiconductor layer, extending from the data line and being separated and spaced apart from the drain electrode.

26. The liquid crystal display device of claim **25**, wherein the first opening portion and the second opening portion of the gate electrode together substantially form a T-shape.

27. The liquid crystal display device of claim **26**, wherein the first opening portion corresponds to the head of the T-shape.

28. The liquid crystal display device of claim **25**, wherein a width of the first opening portion is greater than a width of the second opening portion.

29. The liquid crystal display device of claim **25**, wherein the first electrode of the drain electrode completely overlaps the first opening portion of the gate electrode.

30. The liquid crystal display device of claim **29**, wherein the first electrode of the drain electrode partially overlaps the second opening portion of the gate electrode.

31. The liquid crystal display device of claim **25**, wherein a width of the second electrode of the drain electrode is less than a width of the second opening portion of the gate electrode.

32. The liquid crystal display device of claim **25**, further comprising a pixel electrode and the drain electrode further comprising a third electrode contacting the pixel electrode.

33. The liquid crystal display device of claim **32**, wherein the third electrode contacts the pixel electrode via a contact hole.

34. The liquid crystal display device of claim **32**, wherein the second electrode of the drain electrode connects the first and third electrodes of the drain electrodes.

35. The liquid crystal display device of claim **32**, wherein the second electrode of the drain electrode partially overlaps the second opening portion of the gate electrode.

36. The liquid crystal display device of claim **25**, wherein the source electrode substantially surrounds the first electrode of the drain electrode and the first opening portion of the gate electrode.

37. The liquid crystal display device of claim **36**, wherein the source electrode surrounds a portion of the second electrode of the drain electrode and a portion of the second opening portion of the gate electrode.

* * * * *

EXHIBIT B

US006803984B2

(12) **United States Patent**
Park et al.

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(45) **Date of Patent: Oct. 12, 2004**

(54) **METHOD AND APPARATUS FOR MANUFACTURING LIQUID CRYSTAL DISPLAY DEVICE USING SERIAL PRODUCTION PROCESSES**

(75) Inventors: **Sang Ho Park**, Pusan-kwangyokshi (KR); **Sang Seok Lee**, Taegu-kwangyokshi (KR)

(73) Assignee: **LG.Philips LCD Co., Ltd.**, Seoul (KR)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **10/128,452**

(22) Filed: **Apr. 24, 2002**

(65) **Prior Publication Data**

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(30) **Foreign Application Priority Data**

Feb. 25, 2002 (KR) ..... P 2002-9961

(51) **Int. Cl.**[7] **G02F 1/13**; G02F 1/1339; G02F 1/1341

(52) **U.S. Cl.** **349/187**; 349/153; 349/189; 349/190

(58) **Field of Search** 349/153, 189, 349/190, 187

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Primary Examiner—Tarifur R. Chowdhury
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(57) **ABSTRACT**

A method and apparatus are provided for manufacturing a liquid crystal display device. The method includes the steps of providing at least a first substrate and a second substrate on a single production process line, passing the first and second substrates through a sealing material coating portion of the single production process line in serial order such that a sealing material is coated on the second substrate with the first substrate being passed through the sealing material coating portion without forming a sealing material thereon, passing the first and the second substrates through a liquid crystal dispensing portion of the single production process line in serial order such that liquid crystal is dispensed onto a pixel region of one of the first and second substrates with the other one of the first and second substrates being passed through the liquid crystal dispensing portion without dispensing liquid crystal thereon, and assembling the first substrate with the second substrate to form a liquid crystal panel of at least one liquid crystal display device.

21 Claims, 4 Drawing Sheets

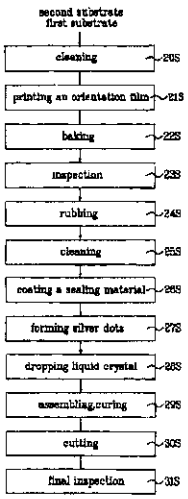

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FIG.1
Related Art

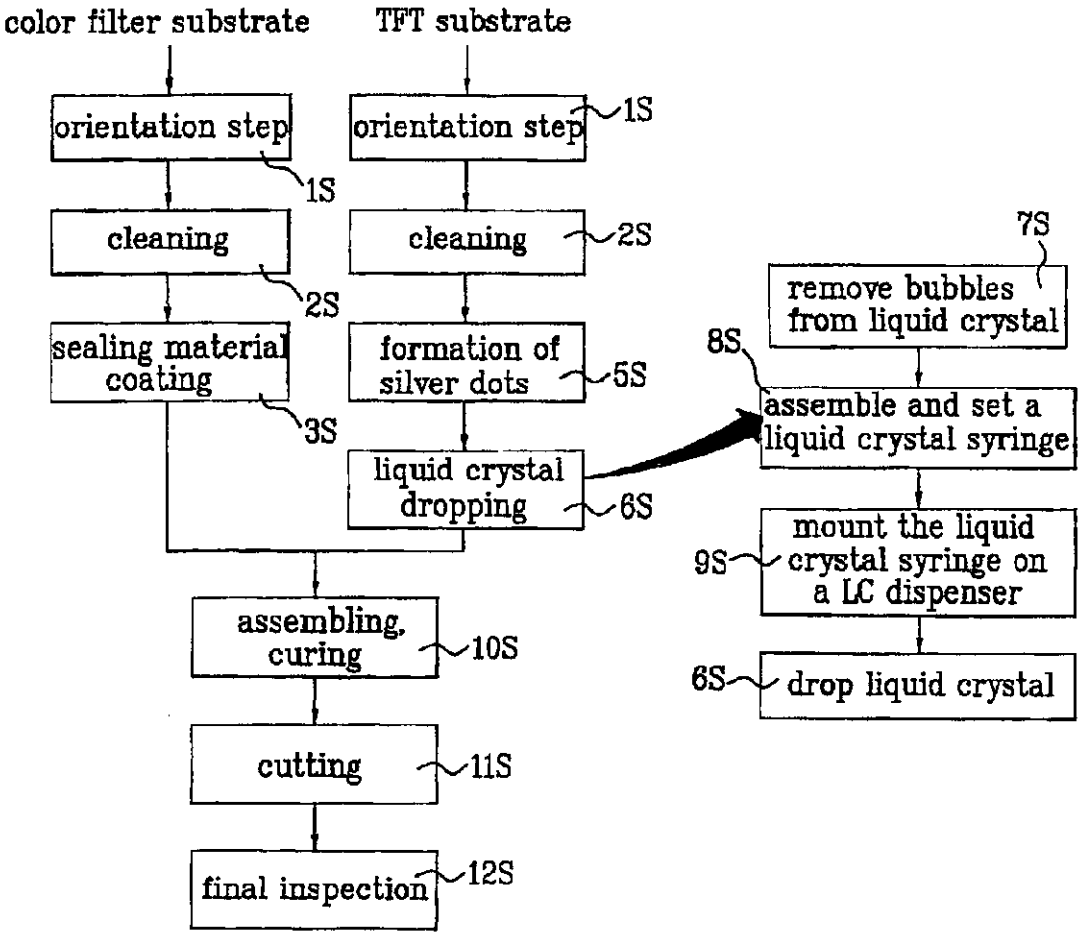
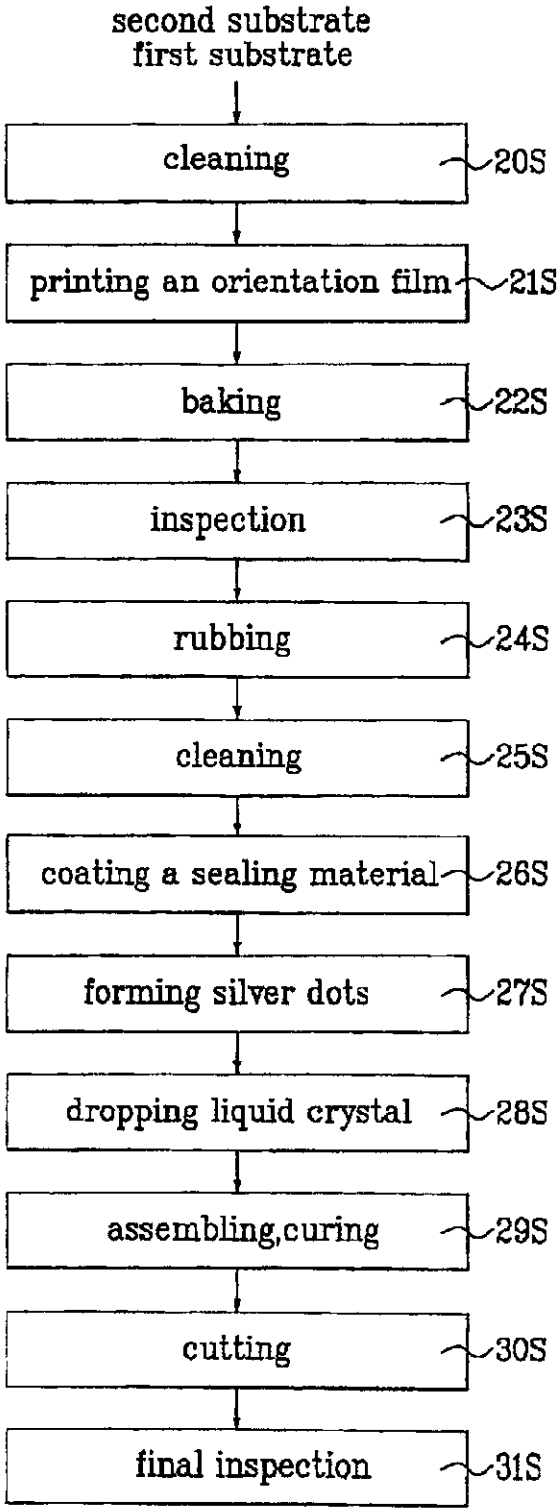


FIG.2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first substrate
cleaning
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printing an orientation film
21S
baking
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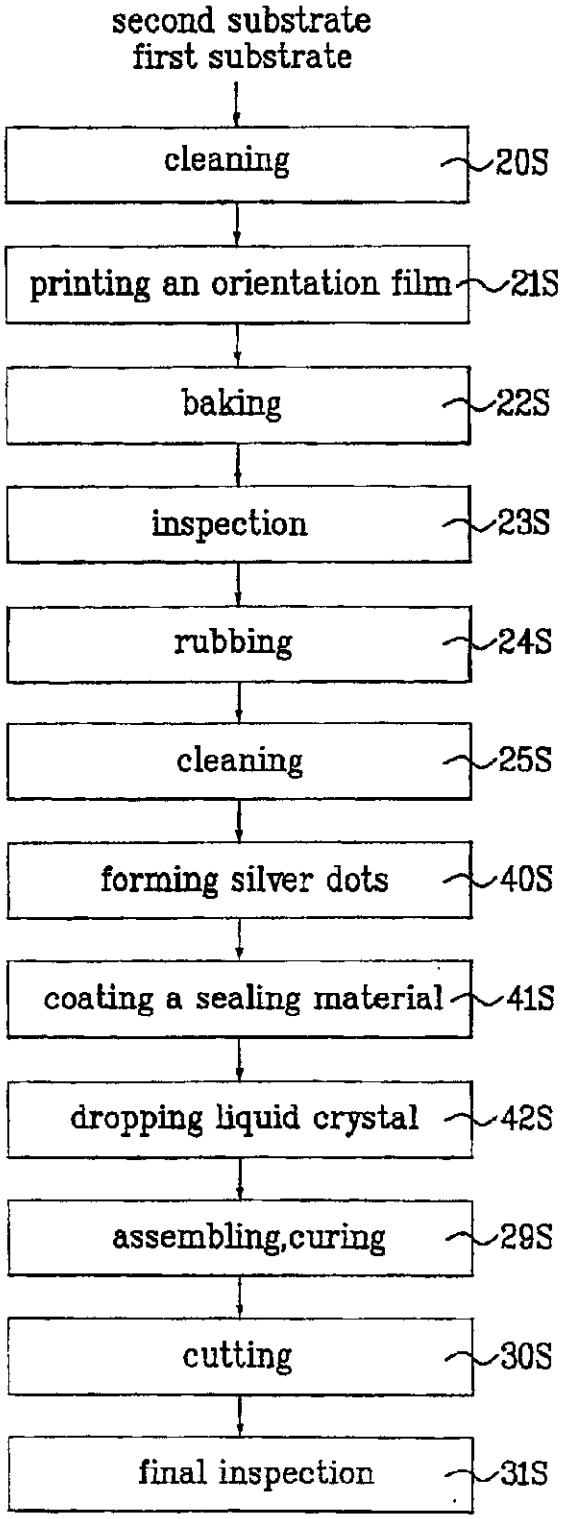
inspection
23S
rubbing
24S
cleaning
25S
coating a sealing material
26S
forming silver dots
27S
dropping liquid crystal
28S
assembling,curing
29S
cutting
30S
final inspection
31S

FIG. 3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assembling,curing
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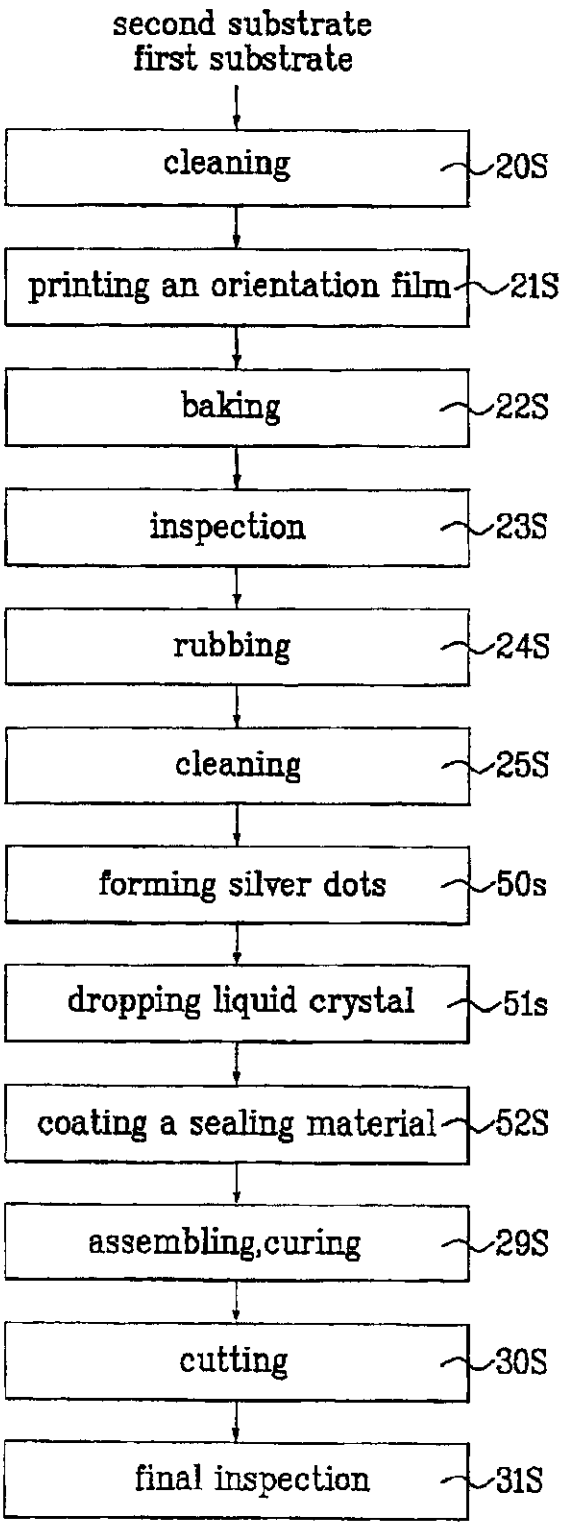
cutting
30S
final inspection
31S

FIG. 4


second substrate
first substrate
cleaning
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inspection
23S
rubbing
24S
cleaning
25S
forming silver dots
50s
dropping liquid crystal
51s
coating a sealing material
52S
assembling,curing
29S
cutting
30S
final inspection
31S

METHOD AND APPARATUS FOR MANUFACTURING LIQUID CRYSTAL DISPLAY DEVICE USING SERIAL PRODUCTION PROCESSES

This application claims the benefit of the Korean Application No. P2002-9961 filed in Korea on Feb. 25, 2002, which is hereby incorporated by reference.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a method and apparatus for manufacturing a liquid crystal display device, and more particularly, to a method and apparatus for manufacturing a liquid crystal display device by using a liquid crystal dropping method.

2. Discussion of the Related Art

With rapid development of an information-oriented society, a need for an information display device having characteristics such as good image quality, light weight, small thickness, and low power consumption has correspondingly been increased. To meet this need, there has been much research directed toward various flat panel display device technologies, such as liquid crystal display device (LCD) technology, plasma display panel (PDP) technology, electro luminescent display (ELD) technology, vacuum fluorescent display (VFD) technology. Some of these display device technologies have already been applied in various applications as the information display device.

Of above various flat panel display devices, the LCD is currently the most widely used due to its ability to meet the above need. In fact, in portable devices such as notebook PC computers, LCD technology has replaced cathode ray tube (CRT) technology. Moreover, even in desktop type displays such as PC monitors and TV monitors, LCD technology has been developed and employed.

A liquid crystal cell includes two opposing substrates and a liquid crystal material filled between the substrates. Liquid crystal is a phase of material having intermediate properties between the liquid and the solid such as fluidity of liquids but long-range order of solids. The liquid crystal material, in an intermediate state between the liquid and the solid, has an optical anisotropy due to its long-range orientational order as well as mechanical fluidity. An LCD is manufactured through a number of processes such as an array process, a color filter process, a liquid crystal cell process, and a module process.

An array process is a process repeating a deposition, a photolithography, and an etching to form a thin film transistor (TFT) array on a first substrate (TFT substrate). A color filter process is a process for forming an ITO (Indium Tin Oxide) film for a common electrode, after red, green, and blue color filters (CF) of dyes or pigments are formed on a second substrate (CF substrate) having a black matrix formed thereon.

A liquid crystal cell process is a process of assembling the TFT substrate and the CF substrate prepared by the array process and the color filter process, respectively. Generally, an empty liquid crystal cell is formed with a fixed and thin gap between the first substrate and the second substrate. Then, the liquid crystal is filled through an opening around the gap to form a liquid crystal panel. A module process is a process for assembling a driving circuit part for processing input and output signals, connecting the liquid crystal panel to a signal processor, and assembling some frames, thereby completing the liquid crystal module.

The step of filling liquid crystal into the liquid crystal cell in the liquid crystal cell process step can be explained as follows.

In the liquid crystal filling step, a liquid crystal material is contained in a container disposed in a chamber. The chamber is maintained in a vacuum state for removing moisture and air dissolved in the liquid crystal material or contained inside the container. While maintaining the vacuum state of the chamber, a liquid crystal filling hole in the empty liquid crystal cell is dipped in the container, and brought into contact with the liquid crystal material. Then, the chamber is vented from a higher vacuum state to a lower vacuum state, and eventually to the atmospheric pressure state. Accordingly, the liquid crystal material is filled into the empty liquid crystal cell through the liquid crystal filling hole by a pressure difference between a pressure in the liquid crystal cell and a pressure in the chamber.

However, the above described liquid crystal filling method has poor productivity because the method needs long time for the liquid crystal filling. That is, before the liquid crystal material is filled into the liquid crystal cell, the large assembled panel must be cut into unit panels, a portion of the unit panel must be dipped into the container, and the liquid crystal filling hole must be brought into contact with the liquid crystal material while the chamber is kept at a vacuum state. Moreover, a large sized LCD is likely to have some defects coming from imperfect filling of the liquid crystal material into the cell.

With regard to this, a liquid crystal dropping method has been developed in which a fixed amount of the liquid crystal is dropped onto an inner surface of the TFT substrate in a corresponding area on the TFT substrate inside a main sealing area formed around the CF substrate (or, alternatively, TFT substrate). Then, the TFT substrate and the CF substrate are assembled into a large liquid crystal panel in a vacuum chamber. The liquid crystal cell process using the liquid crystal dropping method can be explained as follows.

Referring to FIG. **1**, an orientation step (**1S**) in which an orientation material is coated on the TFT substrate and the CF substrate, and mechanical rubbing is carried out on the both substrates for having molecules of the liquid crystal material oriented, carried out. Then, the TFT substrate and the color filter substrate are cleaned (**2S**).

The TFT substrate includes a plurality of gate lines running in one direction at fixed intervals, and a plurality of data lines running in a direction perpendicular to the gate lines at fixed intervals. A plurality of thin film transistors and pixel electrodes are formed in a matrix pixel region defined by the gate lines and the data lines. The CF substrate includes a black matrix layer, a color filter, and a common electrode. Hence, the black matrix layer shields a light leakage of parts except the pixel region.

Then, the cleaned CF substrate is loaded onto a stage of a seal dispenser, and a sealing material is coated on a periphery of the panel (**3S**). The sealing material may be a photo-sensitive resin, or thermo-curing resin. Meanwhile, no filling hole or sealing structure for filling the cell with liquid crystal is required.

At the same time, the cleaned TFT substrate is loaded onto a stage of a silver (Ag) dispenser, and a silver paste material is dotted (i.e., dispensed) into a common voltage supply line of the TFT substrate (**5S**). Then, the TFT substrate is transferred to an LC dispenser, and liquid crystal material is dropped (i.e., dispensed) onto an active array region of each unit panel areas (**6S**). The liquid crystal dropping process is carried out as follows.

After a liquid crystal material is filled into an LC syringe before the LC syringe is assembled and set in the production line, moisture and air dissolved in the liquid crystal material is removed under a vacuum state (7S). Then, the liquid crystal syringe is assembled and set (8S), and mounted on the liquid crystal dispenser (9S). When the TFT substrate is loaded onto a stage of the liquid crystal dispenser, the liquid crystal material is dropped therefrom using the liquid crystal syringe (6S) by dotting a fixed amount of the liquid crystal material onto the TFT substrate at a predetermined pitch inside a coating area of the sealing material (i.e., the pixel region).

After the TFT substrate and the CF substrate are loaded into a vacuum assembling chamber, the TFT substrate and the CF substrate are assembled such that the dropped liquid crystal is uniformly spread over unit panel areas (10S). Then, the sealing material is cured (10S). The assembled TFT substrate and color filter substrate, that is, a large panel, is cut into individual unit panels (11S). Each unit panel is ground and inspected (12S), thereby completing the LCD unit panel.

However, the above method for manufacturing a liquid crystal display having the liquid crystal dropping method applied thereto has the following problems. In the above the liquid crystal cell process, after the orientation steps and the cleaning step, the formation step of silver dots, and the dispensing step of the liquid crystal material on the TFT substrate process, and the sealing material coating step on the CF substrate are carried out using two separate and parallel production lines until the vacuum assembling and curing step (10S). That is, two production lines are used so that the TFT substrate and the CF substrate respectively pass through the orientation step (1S), the cleaning step (2S), the sealing material coating step (3S), the silver dotting step (5S), and the liquid crystal dropping step (6S) in parallel production lines. The use of two production lines results in poor spatial efficiency, higher costs caused by two sets of expensive equipment, and efficiency losses due to different processing times between the two production lines (i.e., line unbalance). Moreover, an inoperative state of one production line caused by failure of the other line reduces productivity substantially.

SUMMARY OF THE INVENTION

Accordingly, the present invention is directed to a method and apparatus for manufacturing a liquid crystal display that substantially obviate one or more of the above problems due to limitations and disadvantages of the related art.

An object of the present invention is to provide a method and apparatus for manufacturing a liquid crystal display, which can maximize spatial efficiency, and improve productivity.

Additional features and advantages of the invention will be set forth in the description which follows, and in part will be apparent from the description, or may be learned by practice of the invention. The objectives and other advantages of the invention will be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

To achieve these and other advantages in accordance with the purpose of the present invention, as embodied and broadly described, a method for manufacturing a liquid crystal display device comprises the steps of providing at least a first substrate and a second substrate on a single production process line; passing the first and second substrates through a sealing material coating portion of the single production process line in serial order, a sealing material being coated on the second substrate with the first substrate being passed through the sealing material coating portion without forming a sealing material thereon; passing the first and the second substrates through a liquid crystal dispensing portion of the single production process line in serial order, liquid crystal being dispensed onto a pixel region of one of the first and second substrates with the other one of the first and second substrates being passed through the liquid crystal dispensing portion without dispensing liquid crystal thereon; and assembling the first substrate with the second substrate to form a liquid crystal panel of at least one liquid crystal display device.

In another aspect, an apparatus for manufacturing a liquid crystal display device having first and second substrates comprises a sealing coating portion disposed to receive the first and second substrates in serial order, the sealing coating portion forming a sealing material on the second substrate and passing the first substrate without forming a sealing material thereon; a liquid crystal dispensing portion in series with the sealing coating portion to receive the first and second substrates in serial order, the liquid crystal dispensing portion dispensing liquid crystal onto one of the first and second substrates and passing the other one of the first and second substrates without dispensing liquid crystal thereon; and an assembler operatively disposed after the sealing coating portion and the liquid crystal dispensing portion, the assembler receiving the first and second substrate and assembling the first substrate with the second substrate to form a liquid crystal panel of a liquid crystal display device.

In another aspect, an apparatus for manufacturing a liquid crystal display device comprises means for providing at least a first substrate and a second substrate on a single production process line; means for passing the first and second substrates through a sealing material coating portion of the single production process line in serial order, a sealing material being coated on the second substrate with the first substrate being passed through the sealing material coating portion without forming a sealing material thereon; means for passing the first and the second substrates through a liquid crystal dispensing portion of the single production process line in serial order, liquid crystal being dispensed onto a pixel region of one of the first and second substrates with the other one of the first and second substrates being passed through the liquid crystal dispensing portion without dispensing liquid crystal thereon; and means for assembling the first substrate with the second substrate to form a liquid crystal panel of a liquid crystal display device.

It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and together with the description serve to explain the principles of the invention. In the drawings:

FIG. 1 is a flow chart illustrating the steps of a method for manufacturing a liquid crystal display device using a related art liquid crystal dropping method;

FIGS. 2–4 are flow charts each illustrating the steps of a method for manufacturing a liquid crystal display device in accordance with exemplary embodiments of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Reference will now be made in detail to the preferred embodiments of the present invention, examples of which are illustrated in the accompanying drawings.

FIGS. **2**–**4** illustrate flow charts each showing the steps of a method for manufacturing a liquid crystal display in accordance with first, second, and third embodiments of the present invention.

Referring to FIG. **2**, a first substrate and a second substrate are provided. The first substrate (hereafter referred to as a "TFT substrate") includes a plurality of gate lines running in one direction at fixed intervals, a plurality of data lines running in a direction perpendicular to the gate lines at fixed intervals, a plurality of thin film transistors, and pixel electrodes in a matrix pixel region defined by the gate lines and the data lines, formed thereon. The second substrate (hereafter referred to as a "color filter substrate") includes a black matrix layer for shielding a light incident to parts except the pixel region, a color filter layer, and a common electrode.

The TFT substrate and the color filter substrate are alternately provided into a production line having a single line structure for progressing the liquid crystal cell process. Processing equipment can be considered as equipment for the TFT substrate, equipment for the color filter substrate or both. The respective substrates are preferably provided to and processed by the corresponding equipment automatically in accordance with information on the substrates.

The liquid crystal cell process will now be explained in detail as follows.

An orientation step is carried out for both of the TFT substrate and the color filter substrate. The orientation step is progressed in an order of cleaning (**20S**) before coating the orientation film, printing of the orientation film (**21S**), baking of the orientation film (**22S**), inspecting of the orientation film (**23S**), and rubbing (**24S**).

After the TFT substrate and the color filter substrate that have passed through the orientation step are cleaned (**25S**), a sealing material is coated onto the color filter substrate, without providing an hole structure for liquid crystal injection so that the color filter substrate can later be assembled with the TFT substrate on a periphery of a pixel region with a fixed gap between the TFT substrate and the color filter substrate (**26S**). In contrast, the TFT substrate passes through the sealing material coating step (**26S**) without coating the sealing material and is provided into the next step.

Silver is coated on the TFT substrate in forms of dots for electrical connection with a common electrode on the color filter substrate (**27S**). However, the color filter substrate passes through the silver coating step (**27S**) without the silver coating and is provided into the next step.

Next, a step for dropping the liquid crystal onto the TFT substrate in a region corresponding to an area inside the sealing material coated on the color filter substrate is carried out (**28S**). Here, the color filter substrate passes through the liquid crystal dropping step (**28S**) without having the liquid crystal dropped thereon, and is provided into the next step.

Of course, it should be recognized that the present invention is not limited to this arrangement. For example, the coating of the sealing material, and the dropping of the liquid crystal material may carried out on either of the TFT substrate or the color filter substrate. The silver dot coating step may be omitted for the production of an IPS (In-Plane Switching) mode LCD in which both the pixel electrode and the common electrode are formed on a single TFT substrate.

Then, the TFT substrate and the color filter substrate are loaded into a vacuum chamber and assembled into a large panel (i.e., a panel having a plurality of LCD unit panels) such that the dropped liquid crystal is spread over the panels uniformly and the sealing material is cured (**29S**).

The large panel, having a TFT substrate and a color filter substrate with liquid crystal therebetween, is cut into individual unit panels (**30S**). Each individual unit panel is ground, and finally inspected (**31S**), thereby completing the manufacturing of an LCD device.

FIGS. **3** and **4** illustrate flow charts showing the steps of a method for manufacturing of a liquid crystal display in accordance with a second and third embodiments of the present invention, respectively, where the order of steps from the sealing material coating step (**26S**) to the liquid crystal dropping step (**28S**) in FIG. **2** are varied.

That is, referring to FIG. **3**, after both the TFT substrate and the color filter substrate passed through the cleaning step (**25S**) of the orientation process, silver is coated on the TFT substrate in form of dots for electrical connection with a common electrode on the color filter substrate (**40S**). However, the color filter substrate passes through the silver coating step (**40S**) without the silver coating and is provided into the next step.

Next, a sealing material is coated on the color filter substrate without providing the liquid crystal filling hole so that the color filter substrate may later be assembled with the TFT substrate on a periphery of a pixel region with a fixed gap between the TFT substrate and the color filter substrate (**41S**). Here, the TFT substrate passes through the sealing material coating step (**41S**) without coating the sealing material thereon and is provided into the next step.

Next, a step for dropping the liquid crystal onto the TFT substrate in a region corresponding to an area inside the sealing material coated on the color filter substrate is carried out (**42S**). However, the color filter substrate passes through the dropping step without having the liquid crystal dropped thereon, and is provided into the next step.

Again, it should be recognized that the present invention is not limited to this arrangement. For example, the coating of the sealing material and the dropping of the liquid crystal may be carried out on either of the TFT substrate or the color filter substrate. The silver dot coating step may be omitted for the production of an IPS mode LCD in which the pixel electrode and the common electrode are formed on a single TFT substrate.

The remaining liquid crystal cell process is finished through the vacuum assembling step of the TFT substrate with the color filter substrate, the curing step of the sealing material (**29S**), cutting (**30S**), and final inspection (**31S**).

Referring to FIG. **4**, after both the TFT substrate and the color filter substrate passed through the cleaning step (**25S**) of the orientation process, silver is coated on the TFT substrate in form of dots for electrical connection with a common electrode on the color filter substrate (**50S**). Here, the color filter substrate passes through the silver coating step without the silver coating and is provided into the next step.

Next, a step for dropping the liquid crystal onto the TFT substrate in a region corresponding to an area inside the sealing material coated on the color filter substrate is carried out (**51S**). Here, the color filter substrate passes through the liquid crystal dropping step without having the liquid crystal dropped thereon, and is provided into the next step.

Next, a sealing material is coated on the color filter substrate without providing a liquid crystal filling hole so that the color filter substrate may later be assembled with the TFT substrate on a periphery of a pixel region with a fixed gap between the TFT substrate and the color filter substrate (52S). However, the TFT substrate passes through the sealing material coating step (52S) without coating the sealing material thereon and is provided into the next step.

Again, it should be recognized that the present invention is not limited to the above arrangement. For example, the coating of the sealing material and the dropping of the liquid crystal may be carried out on either of the TFT substrate or the color filter substrate. The silver dot coating step may be omitted for the production of an IPS mode LCD in which the pixel electrode and the common electrode are formed on a single TFT substrate.

The remaining liquid crystal cell process is finished through the vacuum assembling step of the TFT substrate with the color filter substrate, the curing step of the sealing material (29S), cutting (30S), and final inspection (31S).

Also, it should be recognized that a particular step may be performed on one substrate at the same time that a different step is performed on the other substrate. That is, the production process line receives many thin film transistor substrates and color filter substrates in serial order. Each pair of substrates will pass through each component of the production process line. However, both substrates of each pair need not be disposed in the same component of the production process line at the same time. Thus, one substrate of the pair may be operated on by one component of the production process line at the same time that the other substrate of the pair is being operated on by another component.

As has been explained, the method for manufacturing a liquid crystal display in accordance with the present invention can improve spatial efficiency by adopting a single production line for the liquid crystal cell process, increase the productivity by providing an effective and simple liquid crystal cell process, and can overcome problems caused by a process time difference between the TFT substrate process line and the color filter substrate line. Here, management of respectively providing the TFT substrate and the color filter is simple. Meanwhile, though not shown, the silver dot forming (50S) in the third embodiment may be carried out at a step between the liquid crystal dropping (51S) and the sealing material coating (52S), or after the liquid crystal dropping (51S) and the sealing material coating (52S).

It will be apparent to those skilled in the art that various modifications and variations can be made in the method and apparatus for manufacturing a liquid crystal display of the present invention without departing from the spirit or scope of the invention. Thus, it is intended that the present invention cover the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.

What is claimed is:

1. A method for manufacturing a liquid crystal display device, comprising the steps of:

providing at least a first substrate and a second substrate on a single production process line;

passing the first and second substrates through a sealing material coating portion of the single production process line in serial order, a sealing material being coated on the second substrate with the first substrate being passed through the sealing material coating portion without forming a sealing material thereon;

passing the first and the second substrates through a liquid crystal dispensing portion of the single production process line in serial order, liquid crystal being dispensed onto a pixel region of one of the first and second substrates with the other one of the first and second substrates being passed through the liquid crystal dispensing portion without dispensing liquid crystal thereon; and

assembling the first substrate with the second substrate to form a liquid crystal panel of at least one liquid crystal display device.

2. The method according to claim 1, wherein the sealing material coating portion is provided before the liquid crystal dispensing portion in the single production process line.

3. The method according to claim 1, wherein the liquid crystal dispensing portion is provided before the sealing material coating portion in the single production process line.

4. The method according to claim 1, wherein the liquid crystal is dispensed onto the first substrate.

5. The method according to claim 4, wherein the first substrate is disposed in the liquid crystal dispensing portion and the liquid crystal is dispensed onto the first substrate at the same time that the second substrate is disposed in the sealing material coating portion.

6. The method according to claim 5, wherein the first substrate is a thin film transistor substrate and the second substrate is a color filter substrate.

7. The method according to claim 6, wherein the thin film transistor substrate includes:

a plurality of gate lines running in a first direction at substantially fixed intervals,

a plurality of data lines running in a second direction substantially perpendicular to the gate lines at substantially fixed intervals,

a plurality of thin film transistors and pixel electrodes in a matrix pixel region defined by the gate lines and the data lines, and

an orientation film on the thin film transistors and the pixel electrodes.

8. The method according to claim 6, wherein the color filter substrate includes:

a black matrix layer,

a color filter layer between the black matrix layer for displaying three colors of red, green, and blue,

a common electrode to apply an electric field to the liquid crystal together with the pixel electrodes, and

an orientation film on the common electrode.

9. The method according to claim 1, wherein the liquid crystal is dispensed onto the first substrate, and wherein first substrate is a color filter substrate and the second substrate is a thin film transistor substrate.

10. The method according to claim 1, further comprising the step of cleaning the first substrate and the second substrate in serial order in a same cleaning unit.

11. The method according to claim 1, further comprising the step of cutting the liquid crystal panel into a plurality of unit liquid crystal panels to form a plurality of liquid crystal display devices.

12. The method according to claim 11, further comprising the step of inspecting defects of the unit liquid crystal panels.

13. The method according to claim 1, further comprising a step of passing the first and second substrates through a silver dot forming portion of the single production process line in serial order, silver dots being formed on the first

substrate with the second substrate being passed without forming silver dots thereon.

14. An apparatus for manufacturing a liquid crystal display device having first and second substrates, comprising:

a sealing coating portion disposed to receive the first and second substrates in serial order, the sealing coating portion forming a sealing material on the second substrate and passing the first substrate without forming a sealing material thereon;

a liquid crystal dispensing portion in series with the sealing coating portion to receive the first and second substrates in serial order, the liquid crystal dispensing portion dispensing liquid crystal onto one of the first and second substrates and passing the other one of the first and second substrates without dispensing liquid crystal thereon; and

an assembler operatively disposed after the sealing coating portion and the liquid crystal dispensing portion, the assembler receiving the first and second substrate and assembling the first substrate with the second substrate to form a liquid crystal panel of a liquid crystal display device.

15. The apparatus according to claim **14**, wherein the sealing coating portion is operatively disposed before the liquid crystal dispensing portion.

16. The apparatus according to claim **14**, wherein the liquid crystal dispensing portion is operatively disposed before the sealing coating portion.

17. The apparatus according to claim **14**, wherein the liquid crystal dispensing portion dispenses liquid crystal onto the first substrate, and wherein the first substrate is a thin film transistor substrate and the second substrate is a color filter substrate.

18. The apparatus according to claim **17**, wherein the first substrate is disposed in the liquid crystal dispensing portion at the same time that the second substrate is disposed in the sealing coating portion.

19. The apparatus according to claim **14**, further comprising:

a rubbing unit to mechanically rub, in serial order, the first and second substrates to provide an orientation layer; and

a cleaning unit to clean, in serial order, both the first and second substrates.

20. The apparatus according to claim **14**, further comprising a cutting unit to cut the assembled first and second substrates into a plurality of unit liquid crystal panels.

21. An apparatus for manufacturing a liquid crystal display device, comprising:

means for providing at least a first substrate and a second substrate on a single production process line;

means for passing the first and second substrates through a sealing material coating portion of the single production process line in serial order, a sealing material being coated on the second substrate with the first substrate being passed through the sealing material coating portion without forming a sealing material thereon;

means for passing the first and the second substrates through a liquid crystal dispensing portion of the single production process line in serial order, liquid crystal being dispensed onto a pixel region of one of the first and second substrates with the other one of the first and second substrates being passed through the liquid crystal dispensing portion without dispensing liquid crystal thereon; and

means for assembling the first substrate with the second substrate to form a liquid crystal panel of a liquid crystal display device.

* * * * *

EXHIBIT C

[redacted]

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Park et al.

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(45) **Date of Patent: May 15, 2007**

(54) **LIQUID CRYSTAL DISPLAY DEVICE AND METHOD OF MANUFACTURING THE SAME**

(75) Inventors: **Moo Yeol Park**, Taegu-Kwangyokshi (KR); **Sung Su Jung**, Taegu-Kwangyokshi (KR); **Young Sang Byun**, Kumi-shi (KR)

(73) Assignee: **LG.Philips LCD Co., Ltd.**, Seoul (KR)

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G02F 1/1339 (2006.01)

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(58) **Field of Classification Search** 349/187, 349/189, 190, 191, 153, 154, 155, 156
See application file for complete search history.

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Primary Examiner—Steven S Paik
(74) *Attorney, Agent, or Firm*—McKenna Long & Aldridge LLP

(57) **ABSTRACT**

An LCD device and a method of manufacturing the same are disclosed, in which a sealant concentrated upon the end of a dispensing device is formed in a dummy region on a substrate, so that a liquid crystal layer is not contaminated when both substrates are attached to each other and a cell cutting process can easily be performed. The method of manufacturing an LCD device includes preparing a lower substrate and an upper substrate, forming an auxiliary UV sealant in a dummy region on one of the lower and upper substrate and forming a main UV sealant, applying a liquid crystal on one of the lower and upper substrates, attaching the lower and upper substrates, and irradiating UV light onto the attached substrates.

22 Claims, 9 Drawing Sheets

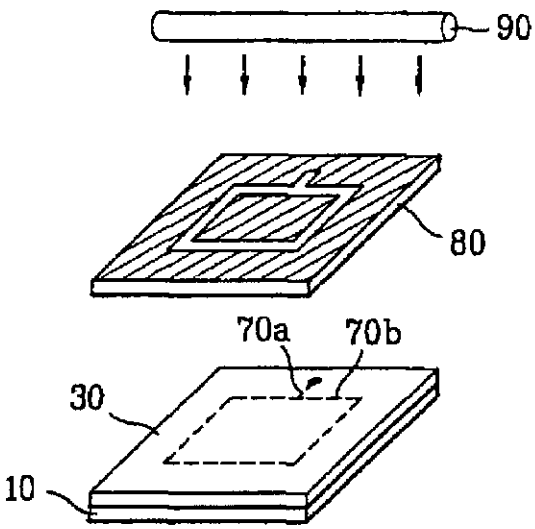

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FIG. 1A
Related Art

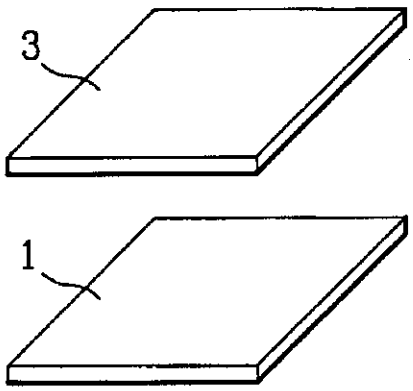


FIG. 1B
Related Art

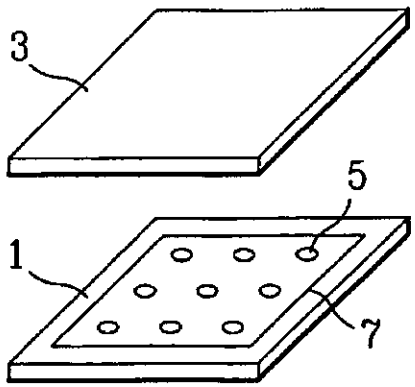


FIG. 1C
Related Art

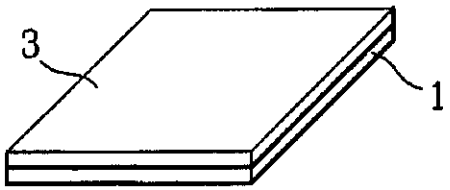


FIG. 1D
Related Art

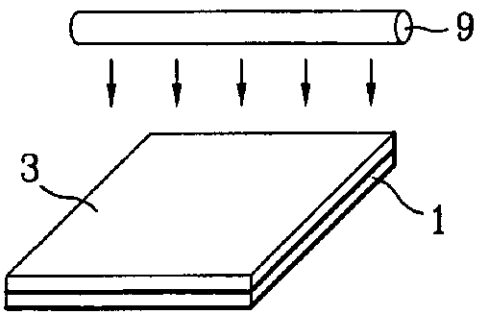


FIG. 2A
Related Art

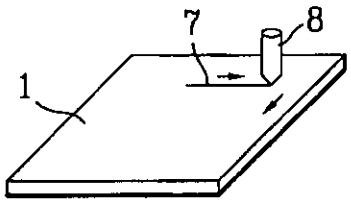


FIG. 2B
Related Art

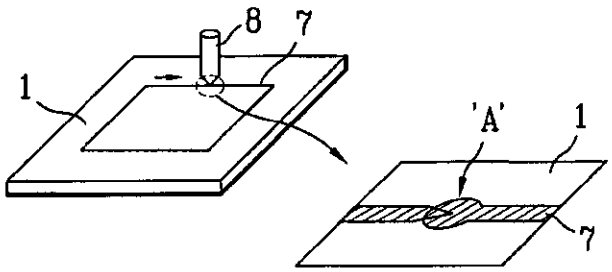


FIG. 2C
Related Art

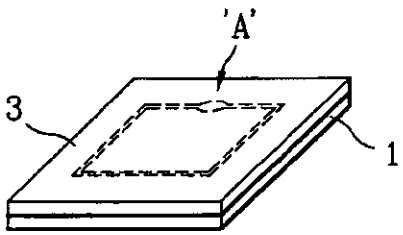


FIG. 3A

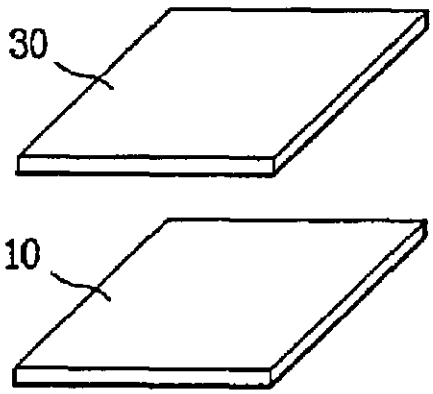


FIG. 3B

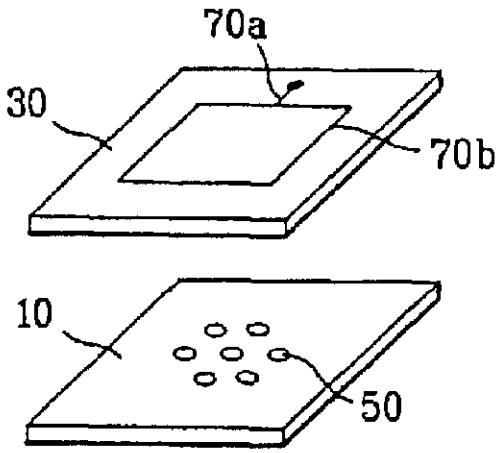


FIG. 3C

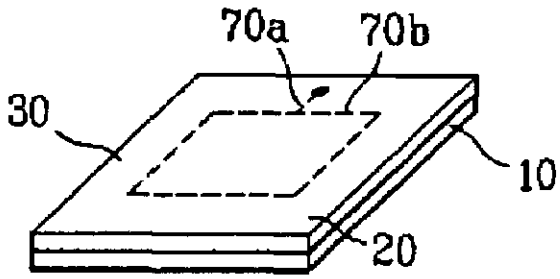


FIG. 3D

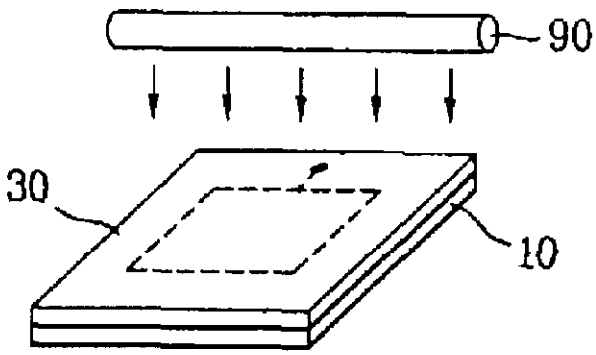


FIG. 4A

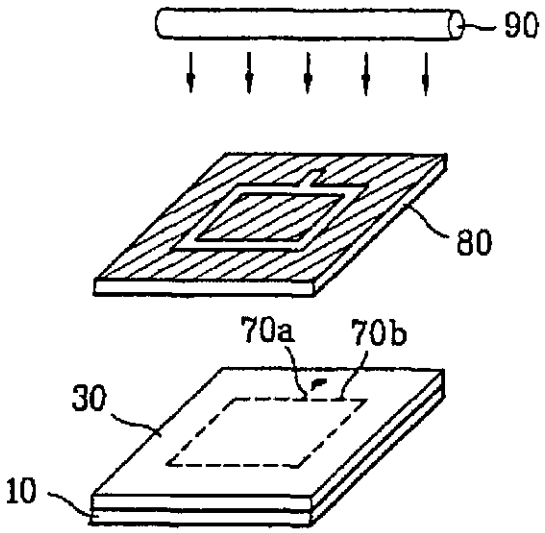


FIG. 4B

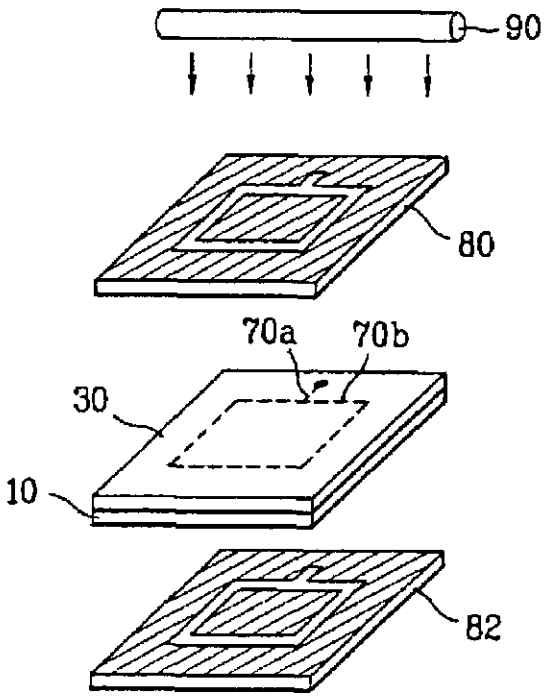


FIG. 4C

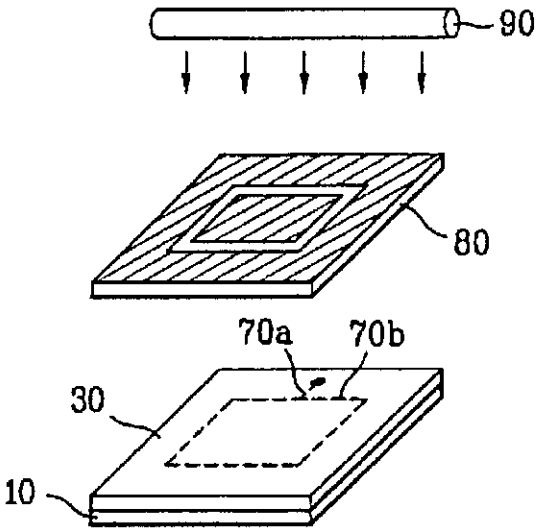


FIG. 4D

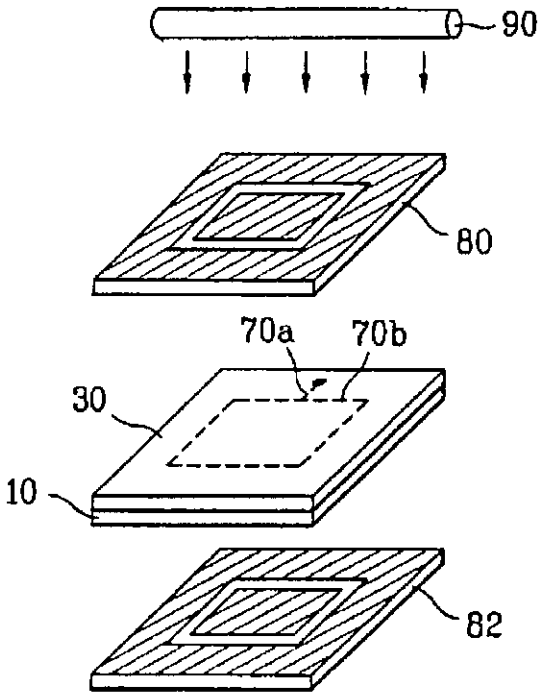


FIG. 5A

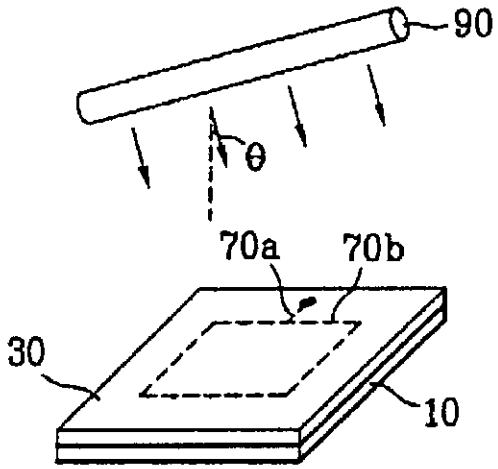


FIG. 5B

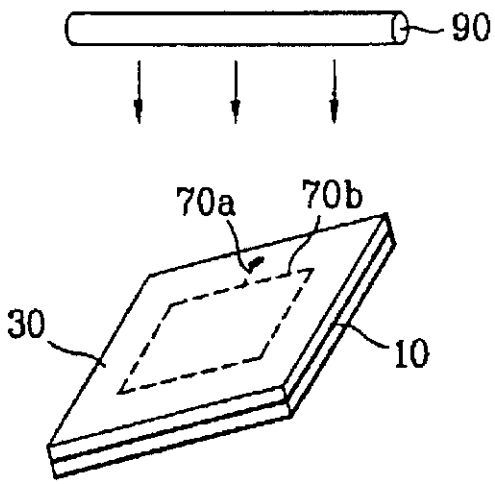


FIG. 6

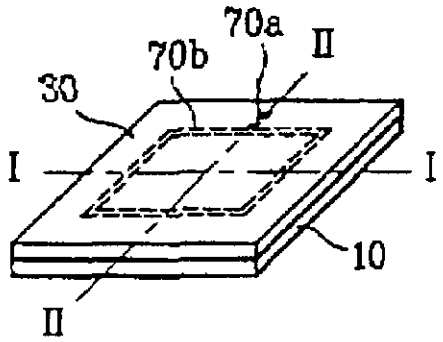


FIG. 7A

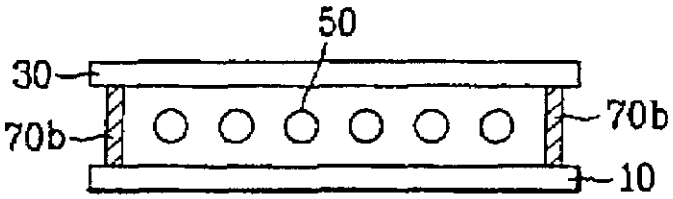
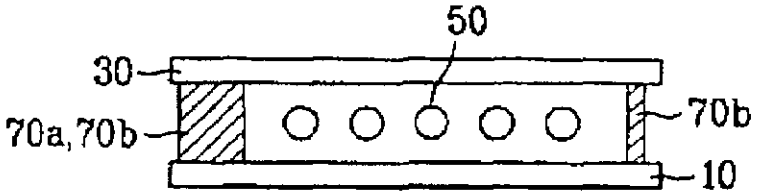


FIG. 7B



LIQUID CRYSTAL DISPLAY DEVICE AND METHOD OF MANUFACTURING THE SAME

This application claims the benefit of the Korean Application No. P2002-8900 filed on Feb. 20, 2002, which is hereby incorporated by reference for all purposes as if fully set forth herein.

This application incorporates by reference two applications, Ser. No. 10/184,096, filed on Jun. 28, 2002, entitled "SYSTEM AND METHOD FOR MANUFACTURING LIQUID CRYSTAL DISPLAY DEVICES"and Ser. No. 10/184,088, filed on Jun. 28, 2002, entitled "SYSTEM FOR FABRICATING LIQUID CRYSTAL DISPLAY AND METHOD OF FABRICATING LIQUID CRYSTAL DISPLAY USING THE SAME", as if fully set forth herein.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a liquid crystal display (LCD) device, and more particularly, to a sealant pattern of an LCD device manufactured by applying a liquid crystal to the surface of a substrate.

2. Discussion of the Related Art

Generally, ultra thin flat panel displays have a display screen with a thickness of several centimeters or less. In particular, flat panel LCD devices are widely used in monitors for notebook computers, spacecraft, and aircraft because such LCD devices have low power consumption and are easy to carry.

Such an LCD device includes a lower substrate, an upper substrate, and a liquid crystal layer. A thin film transistor (TFT) and a pixel electrode are formed on the lower substrate. The upper substrate is formed to oppose the lower substrate. A light-shielding layer, a color filter layer, and a common electrode are formed on the upper substrate. The liquid crystal layer is formed between the lower and upper substrates. In operation an electric field is formed between the lower and upper substrates by the pixel electrode and the common electrode so that the electric field "drives" the alignment of molecules in the liquid crystal layer. Light transmittivity is controlled by driving the liquid crystal layer so that a picture image is displayed.

In the aforementioned LCD device, to form the liquid crystal layer between lower and upper substrates, a vacuum injection method based on capillary phenomenon and pressure difference has been conventionally used. However, such a vacuum injection method has a problem in that it takes long time to inject the liquid crystal into a large display panel, thereby reducing manufacturing productivity.

To solve such a problem, a method of applying liquid crystal on the substrate has been developed and is generally described with reference to FIGS. **1A** to **1D**. Although the drawings illustrate only one unit cell, a plurality of unit cells may be formed depending upon the size of the substrate.

As shown in FIG. **1A**, a lower substrate **1** and an upper substrate **3** are prepared. A plurality of gate and data lines (not shown) are formed on the lower substrate **1**. The gate lines cross the data lines to define a pixel region. A thin film transistor (not shown) is formed at each crossing point between the gate and data lines. A pixel electrode (not shown) connected with the thin film transistor is formed in the pixel region.

A light-shielding layer (not shown) is formed on the upper substrate **3** to prevent light from leaking out from the gate and data lines and the thin film transistor. Color filter layers of red(R), green(G), and blue(B) are formed on the light-shielding layer, and a common electrode is formed on the color filter layers. An alignment film (not shown) is formed on at least one of the lower substrate **1** and the upper substrate **3** to initially align the liquid crystal molecules.

As shown in FIG. **1B**, a sealant **7** is formed on the lower substrate **1** and a liquid crystal **5** is applied thereon, so that a liquid crystal layer is formed. A spacer (not shown) is spread or sprayed onto the upper substrate **3** to maintain a cell gap between the upper and lower substrates.

In the method of manufacturing the LCD device based on the liquid crystal application method, a liquid crystal layer is formed on attached substrates before the sealant **7** is hardened. Therefore, if a thermo-hardening sealant is used as the sealant **7**, the liquid crystal heats and expands so that it flows out of the substrate when it is heated. For this reason, a problem arises in that the liquid crystal **5** is contaminated. Therefore, in the method of manufacturing the LCD based on the liquid crystal application method, a sealant that is at least partially curable by ultraviolet (UV) light is used as the sealant **7**.

The UV sealant is formed by a screen printing method or a dispensing method. In the screen printing method, since a screen comes into contact with the substrate, the alignment film formed on the substrate may be damaged. Also, if the substrate has a large sized area, loss of the sealant increases. In these respects, the dispensing method is preferably used.

As shown in FIG. **1C**, the lower substrate **1** is attached to the upper substrate **3**.

As shown in FIG. **1D**, UV light is irradiated through a UV irradiating device **9** so that the sealant **7** is hardened.

Thereafter, although not shown, a cell cutting process and a final test process are performed, thereby completing a liquid crystal cell.

Meanwhile, FIGS. **2A** and **2B** are perspective views illustrating a process of forming a UV sealant using a dispensing method. In the method of applying liquid crystal to one of the substrates before attaching the the substrates, since no liquid crystal injection hole is required, a sealant **7** having no injection hole is formed on a lower substrate **1** using a dispensing device **8**.

However, since the sealant **7** has high viscosity, it is concentrated upon the end of a nozzle of the dispensing device **8** before the sealant **7** is dispensed. For this reason, a blob "A" of the sealant **7** is excessively deposited at the point where deposition of the sealant **7** on the substrate is started.

As shown in FIG. **2C**, the excessively distributed sealant spreads into an active region (central part of the substrate) and a dummy region (outer part of the substrate) when the lower substrate **1** is attached to the upper substrate **3**. In this case, a problem arises in that the sealant spreads into the active region and contaminates the liquid crystal while the sealant spread out to the dummy region makes the cell cutting process difficult, especially after the sealant is cured.

SUMMARY OF THE INVENTION

Accordingly, the present invention is directed to an LCD device and a method of manufacturing the same that substantially obviates one or more problems due to limitations and disadvantages of the related art.

An advantage of the present invention is to provide an LCD device and a method of manufacturing the same in which a sealant is formed so that a liquid crystal is not contaminated when both substrates are attached to each other and so that a cell cutting process can be easily performed.

Additional advantages and features of the invention will be set forth in part in the description which follows and in part will become apparent to those having ordinary skill in the art upon examination of the following or may be learned from practice of the invention. These and other advantages of the invention may be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

To achieve these and other advantages and in accordance with the purpose of the invention, as embodied and broadly described herein, a method of manufacturing an LCD device according to the present invention includes preparing a lower substrate and an upper substrate; forming an auxiliary sealant and subsequently forming a main sealant on one of the lower and upper substrates, wherein the auxiliary sealant is formed in a dummy region and connect to the main sealant; applying a liquid crystal on one of the lower and upper substrates; attaching the lower and upper substrates; and curing at least the main sealant.

In one embodiment of the present invention, the supplementary UV sealant does not perform the ordinary the function of a sealant, that is, it does not prevent the liquid crystal from leaking out. While the main UV sealant acts as a sealant to confine the liquid crystal.

In another aspect of the present invention, a method of manufacturing a liquid crystal display (LCD) device includes preparing a lower substrate and an upper substrate; forming an auxiliary UV sealant and a main UV sealant on one of the lower and upper substrates, wherein the auxiliary UV sealant is formed in a dummy region and extends from the main UV sealant; applying a liquid crystal on one of the lower and upper substrates; attaching the lower and upper substrates; and irradiating UV light on the attached substrates.

In one aspect of the present invention, the supplementary UV sealant is formed in a dummy region on the substrate and then the closed type main UV sealant is formed, so that the sealant concentrated upon the end of a nozzle of a dispensing device is formed in the dummy region on the substrate.

It is to be understood that both the foregoing general description and the following detailed description of the present invention are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this application, illustrate embodiment(s) of the invention and together with the description serve to explain the principle of the invention.

In the drawings:

FIGS. **1**A to **1**D are perspective views illustrating a method of manufacturing an LCD device according to a related art liquid crystal application method;

FIGS. **2**A and **2**B are perspective views illustrating a process of forming a UV sealant using a related art dispensing method;

FIG. **2**C is a perspective view illustrating a sealant formed by a related art dispensing method after attaching substrates to each other;

FIGS. **3**A to **3**D are perspective views illustrating a method of manufacturing an LCD device according to a first embodiment of the present invention;

FIGS. **4**A to **4**D are perspective views illustrating a process of forming a UV sealant in manufacturing an LCD device according to a second embodiment of the present invention of the present invention;

FIGS. **5**A and **5**B are perspective views illustrating a process of forming a UV sealant in a method of manufacturing an LCD device according to a third embodiment of the present invention of the present invention;

FIG. **6** is a perspective view illustrating an LCD device according to a fourth embodiment of the present invention; and

FIGS. **7**A and **7**B are sectional views taken along lines I—I and II—II of FIG. **6**.

DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENTS

Reference will now be made in detail to the illustrated embodiments of the present invention, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers will be used throughout the drawings to refer to the same or like parts.

FIGS. **3**A to **3**D are perspective views illustrating a method of manufacturing an LCD device according to the first embodiment of the present invention;

Although the drawings illustrate only one unit cell, a plurality of unit cells may be formed depending upon the size of the substrate.

As shown in FIG. **3**A, a lower substrate **10** and an upper substrate **30** are prepared for the process. A plurality of gate and data lines (not shown) are formed on the lower substrate **10**. The gate lines cross the data lines to define a pixel region. A thin film transistor (not shown) having a gate electrode, a gate insulating layer, a semiconductor layer, an ohmic contact layer, source/drain electrodes, and a protection layer is formed at each crossing point of the gate lines and the data lines. A pixel electrode (not shown) connected with the thin film transistor is formed in the pixel region.

An alignment film (not shown) is formed on the pixel electrode to initially align the molecules of liquid crystal. The alignment film may be formed of polyamide or polyimide based compound, polyvinylalcohol (PVA), and polyamic acid by rubbing. Alternatively, the alignment film may be formed of a photosensitive material, such as polyvinvylcinnamate (PVCN), polysilioxanecinnamate (PSCN) or cellulosecinnamate (CelCN) based compound, by using a photo-alignment method.

A light-shielding layer (not shown) is formed on the upper substrate **30** to shield light leakage from the gate lines, the data lines, and the thin film transistor regions. A color filter layer (not shown) of R, G, and B is formed on the light-shielding layer. A common electrode (not shown) is formed on the color filter layer. Additionally, an overcoat layer (not shown) may be formed between the color filter layer and the common electrode. The alignment film is formed on the common electrode.

Silver (Ag) dots are formed outside the lower substrate **10** to apply a voltage to the common electrode on the upper substrate **30** after the lower and upper substrates **10** and **30** are attached to each other. Alternatively, the silver dots may be formed on the upper substrate **30**.

For an in plane switching (IPS) mode LCD, the common electrode is formed on the lower substrate like the pixel electrode, and so that an electric field can be horizontally induced between the common electrode and the pixel electrode. The silver dots are not formed on the substrate.

As shown in FIG. **3**B, a liquid crystal **50** is applied onto the lower substrate **10** to form a liquid crystal layer.

An auxiliary UV curable sealant **70***a* is formed in a dummy area at a corner region of the upper substrate **30**, subsequently, a main UV curable sealant **70***b* having no injection hole is formed, using a dispensing method.

The auxiliary UV sealant **70***a* is prevents any problem that may occur due to a sealant concentrated upon the end of a nozzle of a dispensing device. Therefore, it does not matter where the auxiliary UV sealant **70***a* is formed in the dummy area of the substrate, i.e., any blob of-sealant will be formed away from the active region of the liquid crystal display device and away from a region where the liquid crystal panel will be cut away from the mother substrate assembly. Formation of the main UV sealant **70***b* is preceded by the formation of the auxiliary UV sealant **70***a*. The auxiliary UV sealant **70***a* may be formed in a straight line as shown. Alternatively, the auxiliary UV sealant **70***a* may be formed in a curved line or other shape as long as it is formed in a dummy region.

Monomers or oligomers each having both ends coupled to the acrylic group, mixed with an initiator are used as the UV sealants **70***a* and **70***b*. Alternatively, monomers or oligomers each having one end coupled to the acrylic group and the other end coupled to the epoxy group, mixed with an initiator are used as the UV sealants **70***a* and **70***b*.

Also, the liquid crystal **50** may be contaminated if it comes into contact with the main UV sealant **70***b* before the main UV sealant **70***b* is hardened. Accordingly, the liquid crystal **50** may preferably be applied on the central part of the lower substrate **10**. In this case, the liquid crystal **50** is gradually spread even after the main UV sealant **70***b* is hardened. Thus, the liquid crystal **50** is uniformly distributed on the substrate.

The liquid crystal **50** may be formed on the upper substrate **30** while the UV sealants **70***a* and **70***b* may be formed on the lower substrate **10**. Alternatively, the liquid crystal **50** and the UV sealants **70***a* and **70***b* may be formed on one substrate. In this case, there is an imbalance between the processing times of the substrate with the liquid crystal and the sealants and the substrate without the liquid crystal and the sealants in the manufacturing process. For this reason, the total manufacturing process time increases. Also, when the liquid crystal and the sealants are formed on one substrate, the substrate may not be cleaned even if the sealant contaminates the panel before the substrates are attached to each other.

Accordingly, a cleaning process for cleaning the upper substrate **30** may additionally be provided before the attaching process after the UV sealants **70***a* and **70***b* are formed on the upper substrate **30**.

Meanwhile, spacers may be formed on either of the two substrates **10** and **30** to maintain a cell gap. Preferably, the spacers may be formed on the upper substrate **30**.

Ball spacers or column spacers may be used as the spacers. The ball spacers may be formed in such a manner that they are mixed with a solution having an appropriate concentration and then spread at a high pressure onto the substrate from a spray nozzle. The column spacers may be formed on portions of the substrate corresponding to the gate lines or data lines. Preferably, column spacers may be used for the large sized substrate since the ball spacers may cause an uneven cell gap for the large sized substrate. The column spacers may be formed of a photosensitive organic resin.

As shown in FIG. **3**C, the lower substrate **10** and the upper substrate **30** are attached to each other by the following processes. First, one of the substrates having the liquid crystal dropped thereon is placed at the lower side. The other substrate is placed at the upper side by turning by 180 degrees so that its portion having layers faces into the substrate at the lower side. Thereafter, the substrate at the upper side is pressed, so that both substrates are attached to each other. Alternatively, the space between the substrates may be maintained under the vacuum state so that both substrates are attached to each other by releasing the vacuum state.

Then, as shown in FIG. **3**D, UV light is irradiated upon the attached substrates through a UV irradiating device **90**.

Upon irradiating the UV light, monomers or oligomers activated by an initiator constituting the UV sealants are polymerized and hardened, thereby bonding the lower substrate **10** to the upper substrate **30**.

If monomers or oligomers each having one end coupled to the acrylic group and the other end coupled to the epoxy group, mixed with an initiator are used as the UV sealants, the epoxy group is not completely polymerized by the application of UV light. Therefore, the sealants may have to be additionally heated at about 120° C. for one hour after the UV irradiation, thereby hardening the sealants completely.

Afterwards, although not shown, the bonded substrates are cut into a unit cells and final test processes are performed.

In the cutting process, a scribing process is performed by forming a cutting line on surfaces of the substrates with a pen or wheel of a material having hardness greater than that of glass, such as diamond, and then the substrates are cut along the cutting line by mechanical impact (breaking process). Alternatively, the scribing process and the breaking process may simultaneously be performed using a pen or wheel of a diamond or other hard material.

The cutting line of the cutting process is formed between the start point of the auxiliary sealant, which may be a blob A of sealant, and a main UV sealant across the initially formed auxiliary UV sealant **70***a*. Consequently, a substantial portion of the excessively distributed auxiliary UV sealant **70***a* is removed.

FIGS. **4**A to **4**D are perspective views illustrating a process of irradiating UV light in the method of manufacturing an LCD device according to the second embodiment of the present invention. The second embodiment is similar to the first embodiment except for the UV irradiation process. In the second embodiment, a region where the sealants are not formed is covered with a mask before the UV light is irradiated. Since the other elements of the second embodiment are the same as those of the first embodiment, the same reference numerals will be given to the same elements and their detailed description will be omitted.

If the UV light is irradiated upon the entire surface of the attached substrates, the UV light may deteriorate characteristics of devices such as a thin film transistor on the substrate and may change a pre-tilt angle of an alignment film formed for the initial alignment of the liquid crystal.

Therefore, in the second embodiment of the present invention, the UV light is irradiated when the area where no sealant is formed is covered with a mask.

Referring to FIG. **4**A, a region where the auxiliary UV sealant **70***a* and the main UV sealant **70***b* are formed is covered with a mask **80**. The mask **80** is placed at an upper side of the attached substrates, and the UV light is irradiated.

Also, the mask **80** may be placed at a lower side of the attached substrates. Also, although the UV light is irradiated upon the upper substrate **30** of the attached substrates as shown, the UV light may be irradiated upon the lower substrate **10** by turning the attached substrates.

If the UV light from a UV irradiating device **90** is reflected and irradiated upon an opposite side, it may deteriorate characteristics of devices, such as the thin film transistor on the substrate and the alignment film, as described above. Therefore, masks are preferably formed at lower and upper sides of the attached substrates.

That is, as shown in FIG. **4**B, masks **80** and **82** that cover the region where the sealants **70***a* and **70***b* are not formed are placed are at upper and lower sides of the attached substrates. The UV light is then irradiated thereupon.

Meanwhile, since the auxiliary UV sealant **70***a* does not act as a sealant, it does not require hardening. Also, since the region of the auxiliary UV sealant **70***a* overlaps the cell cutting line during the later cell cutting process, it is more desirable for the cell cutting process that the auxiliary UV sealant **70** is not hardened.

Referring to FIGS. **4**C and **4**D, the auxiliary UV sealant **70***a* is not hardened by irradiating the UV light when only the area where the main UV sealant **70***b* is not formed is covered with the mask, i.e., the auxiliary sealant **70***a* is also covered by a mask.

In this case, in FIG. **4**C, the UV light is irradiated with the mask **80** in place at a lower or upper side of the attached substrates. In FIG. **4**D, the UV light is irradiated when the mask **80** is respectively placed at lower and upper sides of the attached substrates.

FIGS. **5**A and **5**B are perspective views illustrating a process of forming a UV sealant in a method of manufacturing an LCD device according to the third embodiment of the present invention of the present invention.

The third embodiment is identical to the second embodiment except for the UV irradiation process. In the third embodiment, the UV light is irradiated at a tilt angle. Since the other elements of the third embodiment are identical to those of the second embodiment, the same reference numerals will be given to the same elements and their detailed description will be omitted.

If a light-shielding layer and a metal line such as gate and data lines are formed on a region where the UV sealant is formed, the UV light is not irradiated upon the region, thereby failing to harden the sealant. For this reason, adherence between the lower and upper substrates is reduced.

Therefore, in the third embodiment of the present invention, the UV light is irradiated at a tilt angle upon the substrate where the UV sealant is formed, so that the UV sealant is hardened even if the light-shielding layer or the metal line layer is formed between the UV irradiating surface and the sealant.

To irradiate the UV light at a tilt angle, as shown in FIG. **5**A, the attached substrates are horizontally arranged and a UV irradiating device **90** is arranged at a tilt angle of θ. Alternatively, as shown in FIG. **5**B, the attached substrates may be arranged at a tilt angle and the UV irradiating device **90** may horizontally be arranged.

Also, the UV light may be irradiated at a tilt angle when the area where the sealant is not formed is covered with the mask as shown in FIGS. **4**A to **4**D.

FIG. **6** is a perspective view illustrating an LCD device according to the fourth embodiment of the present invention, and FIGS. **7**A and **7**B are sectional views taken along lines I—I and II—II of FIG. **6**.

As shown in FIGS. **6** and **7**, an LCD device according to the present invention includes lower and upper substrates **10** and **30**, a UV sealant between the lower and upper substrates **10** and **30**, having an auxiliary UV sealant **70***a* in a dummy area and a perimeter of main UV sealant **70***b* connected to the auxiliary UV sealant **70***a*, and a liquid crystal layer **50** between the lower and upper substrates **10** and **30**.

At this time, although not shown, a thin film transistor, a pixel electrode, and an alignment film are formed on the lower substrate **10**. A black matrix layer (not shown), a color filter layer (not shown), a common electrode (not shown) and an alignment film (not shown) are formed on the upper substrate **30**. Also, spacers are formed between the lower and upper substrates **10** and **30** to maintain a cell gap between the substrates.

As aforementioned, the LCD device and the method of manufacturing the same according to the present invention have the following advantages.

Since the sealant concentrated upon the end of the nozzle of the dispensing device is formed in the dummy area on the substrate, the liquid crystal layer is not contaminated by the attaching process of the substrates and the cell cutting process is easily performed.

Furthermore, if the UV light is irradiated upon the substrate when the mask is formed at the lower and/or upper side of the attached substrates, the UV light is irradiated upon only the region where the UV sealant is formed. In this case, the alignment film formed on the substrate is not damaged and the characteristics of the devices, such as the thin film transistor, are not deteriorated.

Finally, if the UV light is irradiated at a tilt angle, the sealant can be hardened even if the light-shielding layer or the metal line is formed on the sealant, thereby avoiding reducing adherence between the lower and upper substrates.

It will be apparent to those skilled in the art that various modifications and variations can be made in the present invention. Thus, it is intended that the present invention covers the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.

What is claimed is:

1. A method of manufacturing a liquid crystal display (LCD) device comprising:

preparing a lower substrate and an upper substrate;

forming an auxiliary sealant and subsequently forming a main sealant on one of the lower and upper substrates, wherein the auxiliary sealant is formed in a dummy region and connects to the main sealant, and wherein the auxiliary sealant and the main sealant are contiguous;

applying a liquid crystal on one of the lower and upper substrates;

attaching the lower and upper substrates; and

curing at least the main sealant.

2. The method of claim **1**, wherein the main sealant and the auxiliary sealant are at least partially curable by irradiating UV light and curing the main sealant includes irradiating UV light.

3. The method of claim **2**, wherein the sealant is formed using oligomers each having both ends coupled to an acrylic group.

4. The method of claim **2**, wherein the sealant is formed using monomers each having both ends coupled to an acrylic group.

5. The method of claim **2**, wherein the sealant is formed using oligomers each having one end coupled to an acrylic group and the other end coupled to an epoxy group.

6. The method of claim **5**, further comprising heating the sealant after irradiating the UV light.

7. The method of claim **2**, wherein the sealant is formed using monomers each having one end coupled to an acrylic group and the other end coupled to an epoxy group.

8. The method of claim 7, further comprising heating the sealant after irradiating the UV light.

9. The method of claim 2, further comprising heating the sealant after irradiating the UV light.

10. The method of claim 2, wherein a region where the sealant is not formed is covered with a mask during the irradiating with UV light.

11. The method of claim 2, wherein a region where the main UV sealant is not formed is covered with a mask during the irradiating with UV light.

12. The method of claim 2, wherein the UV light is irradiated at a tilt angle with respect to the attached substrates.

13. The method of claim 2, further comprising:

providing a mask over a region where the main sealant is not formed before irradiating UV light such that the auxiliary sealant is not exposed to the UV light; and

cutting the attached substrates.

14. The method of claim 1, further comprising forming column spacers on the upper substrate.

15. The method of claim 1, wherein the main and auxiliary sealants are formed on the upper substrate and the liquid crystal is applied to the lower substrate.

16. The method of claim 1, further comprising cutting the attached substrates.

17. The method of claim 16, wherein the attached substrates are cut across a portion of the auxiliary sealant.

18. The method of claim 1, wherein the applying the liquid crystal includes dropping the liquid crystal onto the one of the upper and lower substrates.

19. The method of claim 18, wherein the liquid crystal is applied in a predetermined pattern onto the one of the upper and lower substrates.

20. The method of claim 1, wherein the auxiliary sealant contacts the main sealant.

21. A method of manufacturing a liquid crystal display (LCD) device comprising:

preparing a lower substrate and an upper substrate;

forming an auxiliary UV sealant and a main UV sealant on one of the lower and upper substrates, wherein the auxiliary UV sealant is formed in a dummy region and extends outside from the main UV sealant, wherein the auxiliary UV sealant contacts the main UV sealant;

applying a liquid crystal on one of the lower and upper substrates;

attaching the lower and upper substrates; and

irradiating UV light on the attached substrates.

22. The method of claim 21, wherein the UV light is irradiated at a tilt angle with respect to the attached substrates.

* * * * *